ALINX FPGA BOARD

AX7103

User Manual

ALINX

Revsion History:

Revision	Description
1.0	First Release

Development Environment:
Vivado 2017.4 is from Xilinx website
https://www.xilinx.com

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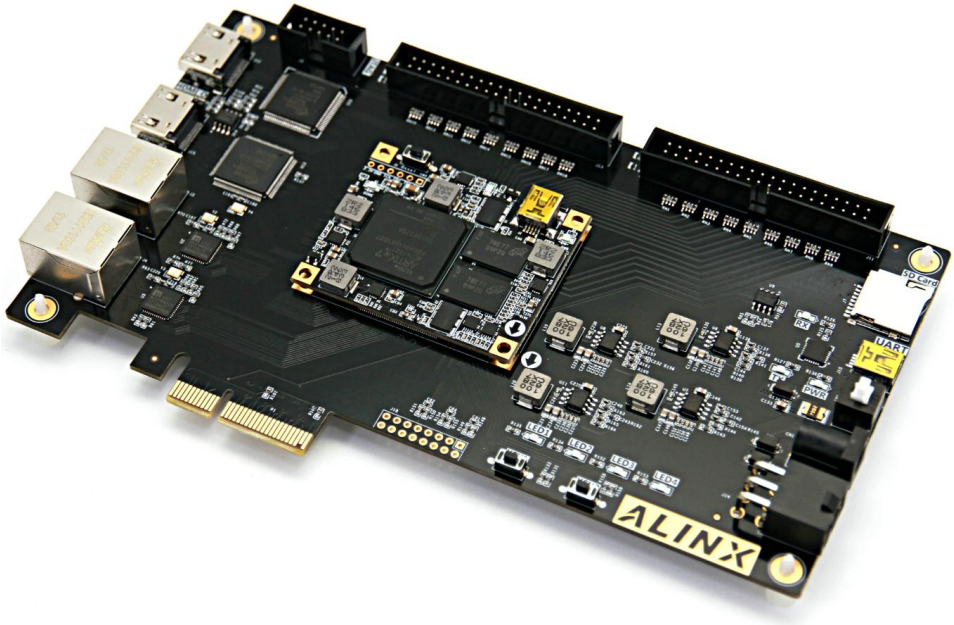
Contents

Overview

The ALINX ARTIX-7 FPGA Development board now released officially (module number: AX7103). In order to learn the FPGA board quickly, we write this manual for user.

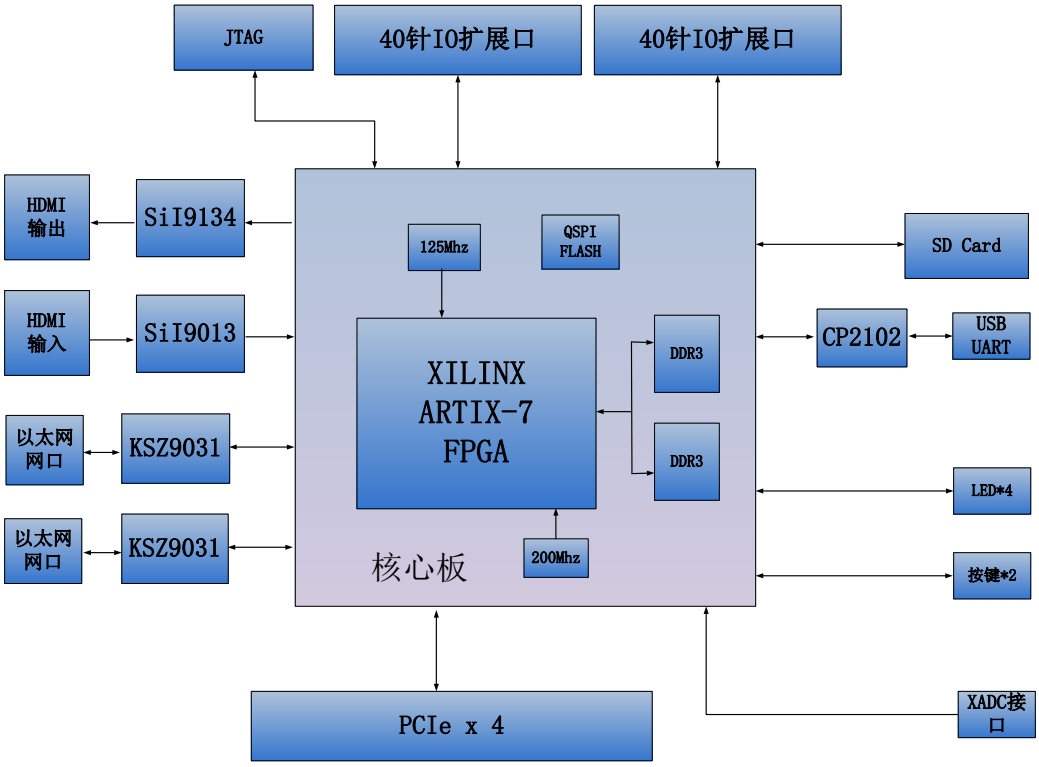
The ARTIX-7 FPGA development platform includes core board and expansion board, so that users can reuse the core board in their own projects conveniently. The kit contains complete reference designs and source code for each part on board. It is a good choice for students or FPGA engineers to learn Artix-7 FPGA and do evaluation base on it. This document provides users key information about the kit. Figure1-1 shows a photograph of the whole board.



The AX7103 board comprised FPGA core board and expansion board, four high-speed board-to-board connectors are used to connect between the core board and the expansion board

The core board is a minimal system which mainly consists of FPGA chipset, two DDR3 and QSPI FLASH. The expansion board extends many peripheral interfaces for core board, which contains PCIex4 connector, gigabit Ethernet network port, HDMI input, HDMI output, UART serial connector, SD socket, XADA connector, 2 pairs of 40-pin connector header and etc.

Below schematic diagram provides a quick overview of AX7103 board.



Judge from the schematic diagram above, the AX7103 Development board could achieve the below functions.

Artix-7 FPGA Core

The core board consists of XC7A100T+8Gb DDR3+128Mb QSPI FLAS, two high resolution LVDS differential crystals of Sitime company, one is 200MHz used to FPGA System, another is 125MHz to provide stable clock input for GTP modules.

PCIe x4 connector

Support PCI Express 2.0 standard, provide PCIe x4 High-speed data transmission interface, single channel communication speed up to 5GBaud。

10/100M/1000M Ethernet RJ-45 connector

Gigabit Ethernet connector chip, that use KSZ9031RNX Ethernet PHY chip of Micrel company, provide network communication services for user. Support 10/100/1000 Mbps network transmission rate; Full duplex and adaptive

HDMI Output

SIL9134 HDMI code chip of Silicon Image Company, support up to 1080P@60Hz output, support 3D output。

HDMI Inupt

SIL9013 HDMI decode chip of Silion Image company, support up to 1080P@60Hz input, and support date output in different format

USB Uart connector

One Uart transfer to USB connector, that used to communication with computer, easy to debug. Serial chip USB-UAR of Silicon Labs CP2102GM, MINI USB connector

Micro SD socket

One Micro SD socket, support SD mode and SPI mode

EEPROM

One chip EEPROM 24LC04 of IIC connector on board

2 pairs of 40-pin expansion header

Reserved 2 pairs 2.54mm standard spacing 40-pin expansion header. They used to connect all kinds of AXSOC modules or outside circuit designed by users. There are 40pins for every expansion header, and one pin for 5V power supply, 2 pins for 3.3V power supply, 3 pins for ground, the other 34pins for IOs. Do not connected IOs to 5V circuit directly, or may damage the FPGA, if to connect, that need through level convert chip

JTAG Connector

10 pins 2.54mm standard JTAG Connectors, that use to download and debug the FPGA program

2 Buttons

2 user Buttons (one button acts as reset button on core board)

LED Light

5 User LEDs and (one is on core board, four are on expansion board)

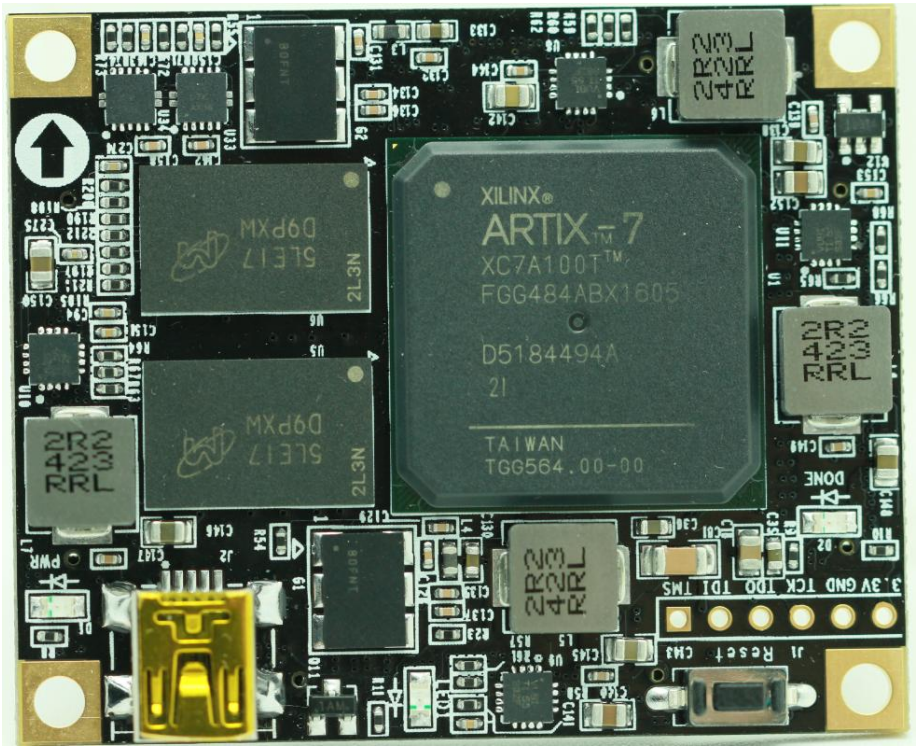
FPGA Core Board

1. Overview

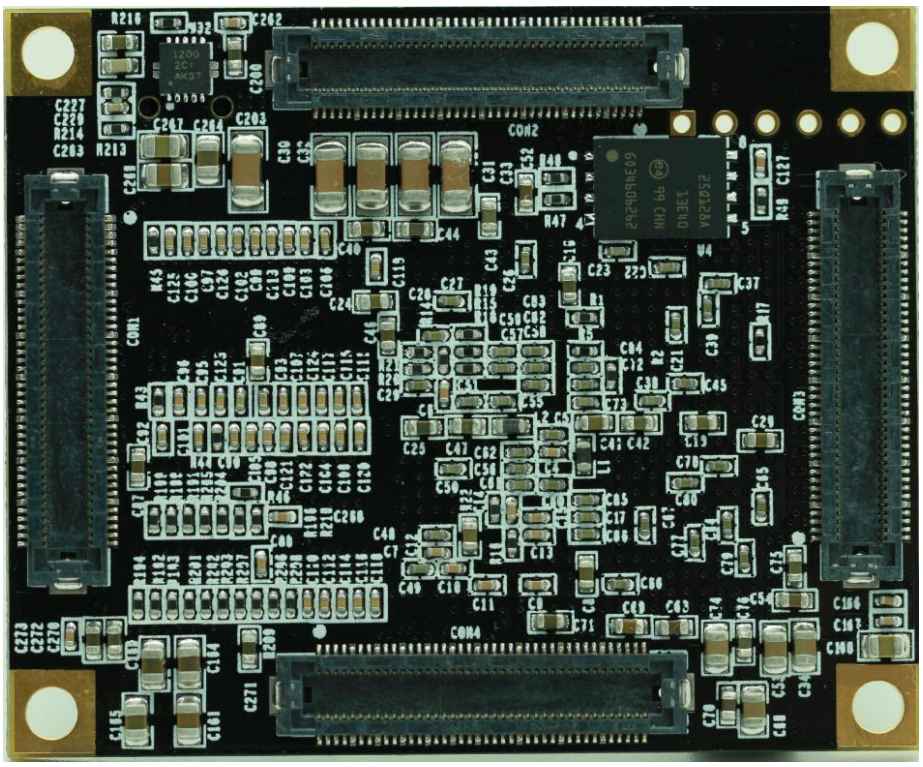
AC7100 (module number of Core Board) core board, is a high performance core board using XILINX Artix-7 XC7A100T-2FGG484I chipset. Two DDR3 memories are connected to FPGA with 32bit data width and one 128Mbit QSPI FLASH is used for storage of FPGA bitstreams or application code.

About 180 IOs (include 86 pairs LVDS signals) and signals of GTP transceivers are extended to expansion board using board-on-board connector. The core board is very small of 45*55 (mm), it will be a good choice to use this core board in project which need a lot of IOs and space limitation

Figure 2-1-1 and Figure 2-1-2 shows the top view and bottom view of the FPGA Core board.



AC7100 Top View



AC7100 Bottom view

2. FPGA

AC7100 Core board uses Xilinx Artix-7 FPGA device, the detail part number is **XC7A100T-2FGG484I.** Speed grade is 2, Temperature grade is industrial. The Xilinx Artix-7 FPGA ordering information is shown in Figure 2-2-1.

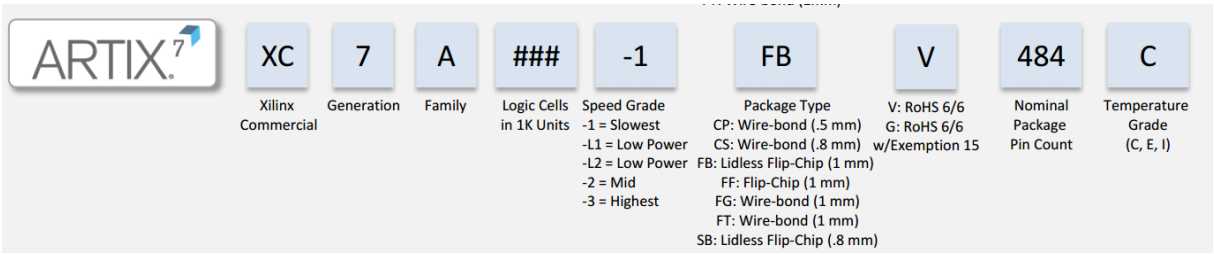


Figure 2-2-1 Artix-7 Ordering Information

Figure 2-2-1 FPGA chip

The feature summary of XC7A100T is listed as below

Items	Parameters
Logic Cells	101440
Slices	15850
CLB flip-flops	126800
Block RAM（kb）	4860
DSP Slices	240
PCIe Gen2	1
XADC	1 is 12bit, 1Mbps AD
GTP Transceiver	4,6.6Gb/s max
Speed grade	-2
Temperature Grade	Industrial

FPGA Power Supply

Artix-7 FPGA has six power supplies including V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCO}, $V_{MGTAVCC}$ and $V_{MGTAVTT}$. V_{CCINT} is the core power supply of FPGA and should be connected to +1.0V. V_{CCBRAM} is power supply of FPGA Block RAM and also should be connected to +1.0V. V_{CCAUX} is FPGA auxiliary power supply and should be connected to +1.8V. V_{CCO} is each BANK power supply, because the IOs of FPGA bank35 is connected to the DDR3, the V_{CCO} voltage of bank35 should be +1.5V. V_{CCO} of Bank15 and Bank16 is power from a LDO chipset, so the voltage of these two Bank can be changed if we use different LDO chipset. $V_{MGTAVCC}$ is the power supply of GTP transceiver, it should be connected to +1.0V. $V_{MGTAVTT}$ is terminal power supply of the GTP transceiver, and should be connected to the +1.2V

Artix-7 FPGA has the Power-On/Off Power supply sequencing, the recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The

recommended power-off sequence is the reverse of the power-on.

3. Differential Crystal Oscillator

AC7100 core board is equipped with two Sitime differential crystal oscillators , one is 200Mhz differential crystal oscillator for FPGA system clock, another is 148.5Mhz differential crystal oscillator for GTP transceiver reference.

1). 200Mhz Differential Crystal Oscillator

The Figure 2-3-1 is the circuit of 200Mhz system clock, the output of differential crystal oscillator is connected to global clock pin MRCC (R4 and T4) of FPGA. The 200Mhz system clock can produce different frequency clock to drive the user logic thought PLLs and DCMs inside FPGA.

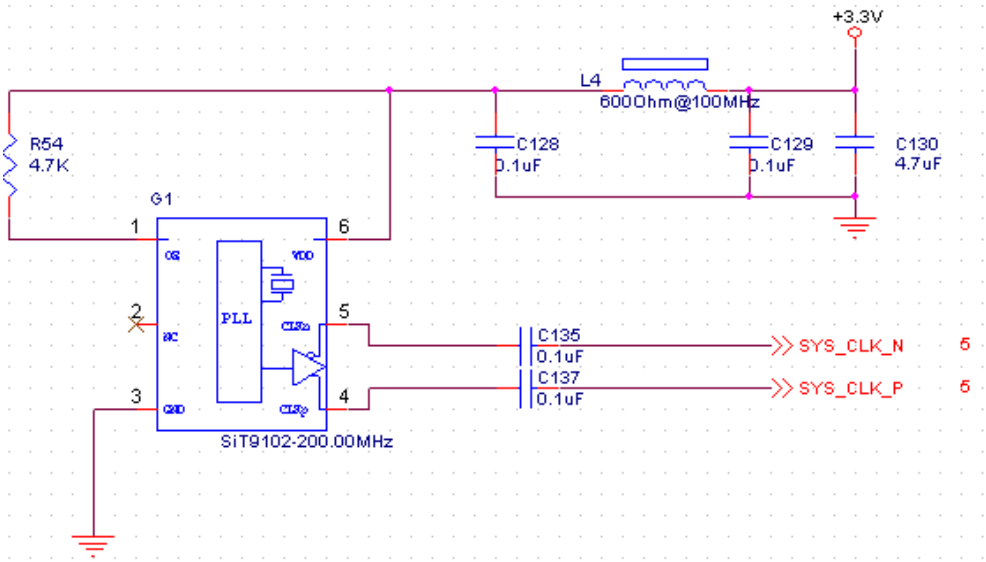


Figure 2-3-1 200Mhz Differential Crystal Oscillator

Figure 2-3-2 is 200Mhz Differential Crystal Oscillator on board.

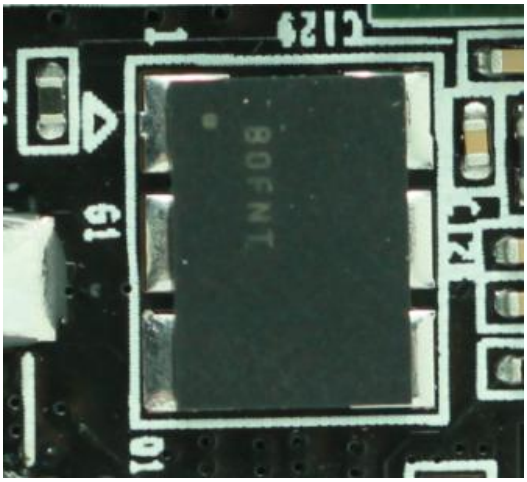


Figure 2-3-2 200Mhz Differential Crystal Oscillator

Pin Assignment of Clock：

Net Name	FPGA PIN
SYS_CLK_P	R4
SYS_CLK_N	T4

2). 125Mhz Differential Clock

The differential crystal oscillator marked as G2 in Figure 2-3-3, used to provide the reference input clock to GTP modules in FPGA. The Figure 2-3-3 is the circuit of 125Mhz clock for GPT transceiver. The output of differential crystal oscillator is connected to MGTREFCLK0P pin (F6) and MGTREFCLK0N pin (E6) of FPGA.

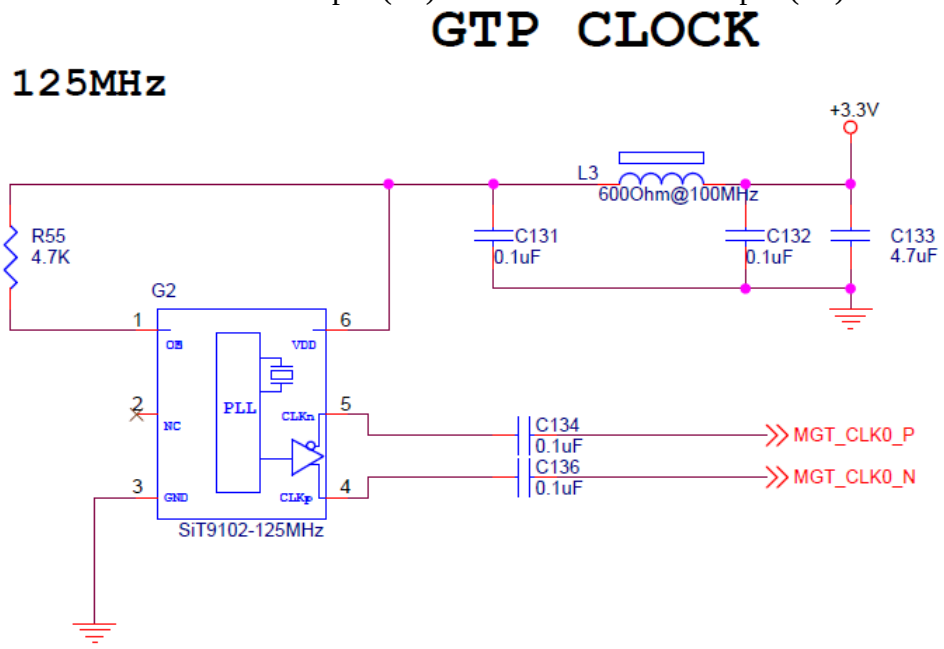


Figure 2-3-3 125Mhz Differential Crystal Oscillator

Figure 2-3-4 is 为125M Differential Active Crystal Oscillator

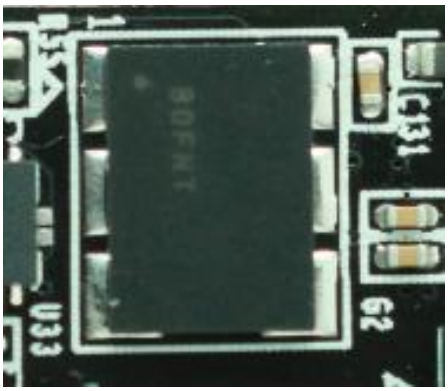


Figure2-3-4 125M Oscillator on board

Pin assignment of Clock：

Net Name	FPGA PIN
MGT_CLK0_P	F6
MGT_CLK0_N	E6

4. DDR3

The core board features 4GB of DDR3 memory, implemented using four 512MB DDR3 devices. The data bandwidth is in 32-bit, comprised of two x16 devices with a single address/command bus. The target clock speed for FPGA and DDR3 is 800 MHz (Data rate is 1600M). The part number of equipped two DDR3 devices is Micron MT41J256M16HA-125 which is compatible with

MT41K256M16HA-125. The DDR3 memory system connected to the memory connector of BANK 34 and BANK 35 in FPGA. Detail information of DDR3 SDRAM is shown in table 2-4-1 below

Table 2-4-1 DDR3 SDRAM Configuration

Part	P/N	Capacity	Vender
U5,U6	MT41J256M16HA-125	256M x 16bit	micron

The hardware design of DDR3, considered the signal integrity strictly. During hardware circuit and PCB designation, we consider the register match/ terminal register/, control the line impedance and length, that all to make sure DDR work high speed stable.

Connection between FPGA and DDR3 are shown in Figure2-4-1

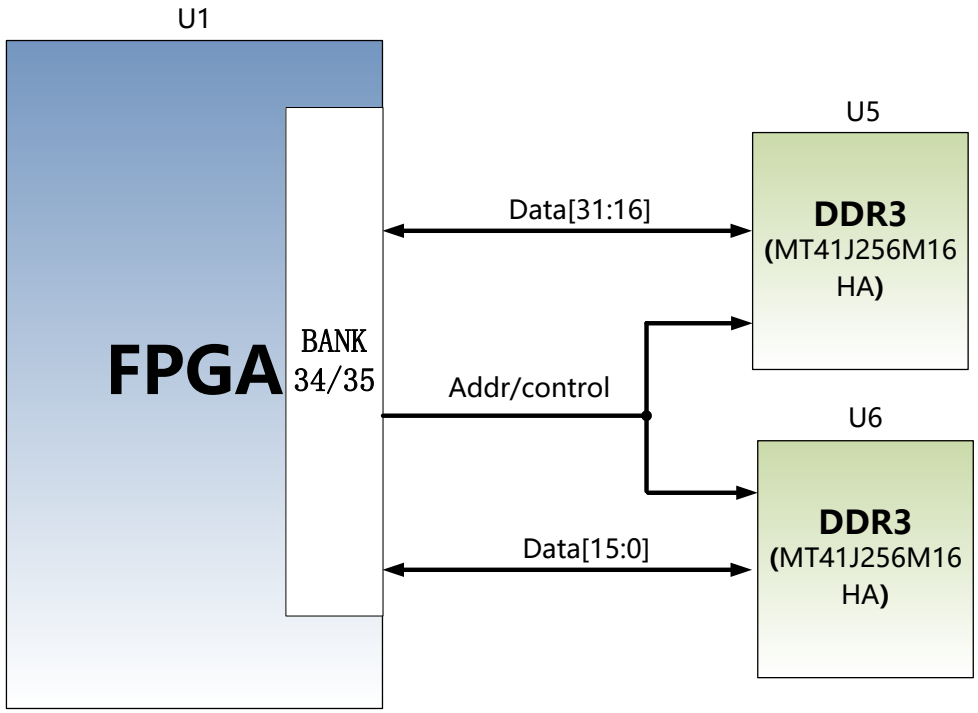


Figure 2-4-1 DDR3 DRAM Schematic

Figure 2-4-2 is DDR3 DRAM on board.

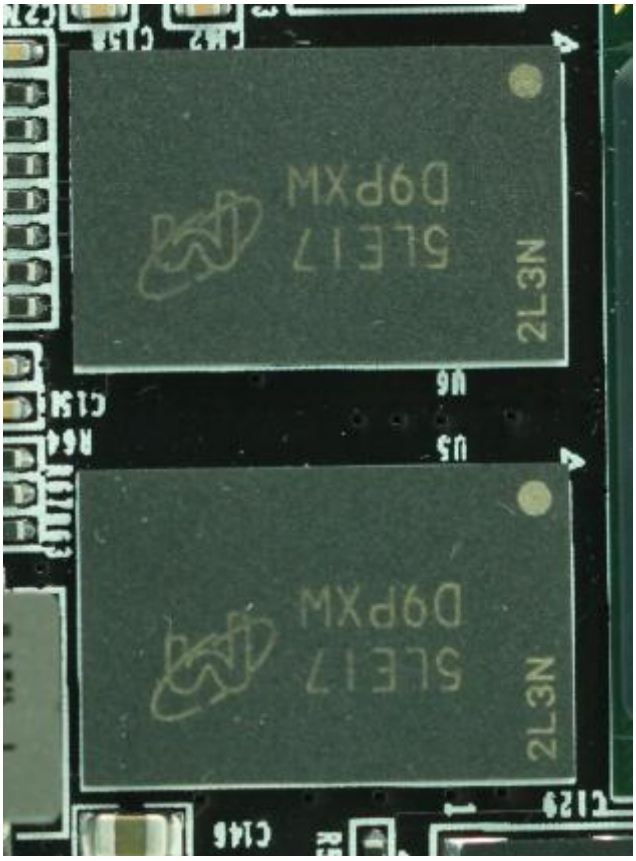


Figure 2-4-2 DDR3 DRAM on board

Pin Assignment of DDR3 DRAM：

Net Name	FPGA PIN Name	FPGA P/N
DDR3_DQS0_P	IO_L3P_T0_DQS_AD5P_35	E1
DDR3_DQS0_N	IO_L3N_T0_DQS_AD5N_35	D1
DDR3_DQS1_P	IO_L9P_T1_DQS_AD7P_35	K2
DDR3_DQS1_N	IO_L9N_T1_DQS_AD7N_35	J2
DDR3_DQS2_P	IO_L15P_T2_DQS_35	M1
DDR3_DQS2_N	IO_L15N_T2_DQS_35	L1
DDR3_DQS3_P	IO_L21P_T3_DQS_35	P5
DDR3_DQS3_N	IO_L21N_T3_DQS_35	P4
DDR3_DQ[0]	IO_L2P_T0_AD12P_35	C2
DDR3_DQ [1]	IO_L5P_T0_AD13P_35	G1
DDR3_DQ [2]	IO_L1N_T0_AD4N_35	A1
DDR3_DQ [3]	IO_L6P_T0_35	F3
DDR3_DQ [4]	IO_L2N_T0_AD12N_35	B2
DDR3_DQ [5]	IO_L5N_T0_AD13N_35	F1
DDR3_DQ [6]	IO_L1P_T0_AD4P_35	B1
DDR3_DQ [7]	IO_L4P_T0_35	E2
DDR3_DQ [8]	IO_L11P_T1_SRCC_35	H3
DDR3_DQ [9]	IO_L11N_T1_SRCC_35	G3

DDR3_DQ [10]	IO_L8P_T1_AD14P_35	H2
DDR3_DQ [11]	IO_L10N_T1_AD15N_35	H5
DDR3_DQ [12]	IO_L7N_T1_AD6N_35	J1
DDR3_DQ [13]	IO_L10P_T1_AD15P_35	J5
DDR3_DQ [14]	IO_L7P_T1_AD6P_35	K1
DDR3_DQ [15]	IO_L12P_T1_MRCC_35	H4
DDR3_DQ [16]	IO_L18N_T2_35	L4
DDR3_DQ [17]	IO_L16P_T2_35	M3
DDR3_DQ [18]	IO_L14P_T2_SRCC_35	L3
DDR3_DQ [19]	IO_L17N_T2_35	J6
DDR3_DQ [20]	IO_L14N_T2_SRCC_35	K3
DDR3_DQ [21]	IO_L17P_T2_35	K6
DDR3_DQ [22]	IO_L13N_T2_MRCC_35	J4
DDR3_DQ [23]	IO_L18P_T2_35	L5
DDR3_DQ [24]	IO_L20N_T3_35	P1
DDR3_DQ [25]	IO_L19P_T3_35	N4
DDR3_DQ [26]	IO_L20P_T3_35	R1
DDR3_DQ [27]	IO_L22N_T3_35	N2
DDR3_DQ [28]	IO_L23P_T3_35	M6
DDR3_DQ [29]	IO_L24N_T3_35	N5
DDR3_DQ [30]	IO_L24P_T3_35	P6
DDR3_DQ [31]	IO_L22P_T3_35	P2
DDR3_DM0	IO_L4N_T0_35	D2
DDR3_DM1	IO_L8N_T1_AD14N_35	G2
DDR3_DM2	IO_L16N_T2_35	M2
DDR3_DM3	IO_L23N_T3_35	M5
DDR3_A[0]	IO_L11N_T1_SRCC_34	AA4
DDR3_A[1]	IO_L8N_T1_34	AB2
DDR3_A[2]	IO_L10P_T1_34	AA5
DDR3_A[3]	IO_L10N_T1_34	AB5
DDR3_A[4]	IO_L7N_T1_34	AB1
DDR3_A[5]	IO_L6P_T0_34	U3
DDR3_A[6]	IO_L5P_T0_34	W1
DDR3_A[7]	IO_L1P_T0_34	T1
DDR3_A[8]	IO_L2N_T0_34	V2
DDR3_A[9]	IO_L2P_T0_34	U2
DDR3_A[10]	IO_L5N_T0_34	Y1
DDR3_A[11]	IO_L4P_T0_34	W2
DDR3_A[12]	IO_L4N_T0_34	Y2
DDR3_A[13]	IO_L1N_T0_34	U1

DDR3_A[14]	IO_L6N_T0_VREF_34	V3
DDR3_BA[0]	IO_L9N_T1_DQS_34	AA3
DDR3_BA[1]	IO_L9P_T1_DQS_34	Y3
DDR3_BA[2]	IO_L11P_T1_SRCC_34	Y4
DDR3_S0	IO_L8P_T1_34	AB3
DDR3_RAS	IO_L12P_T1_MRCC_34	V4
DDR3_CAS	IO_L12N_T1_MRCC_34	W4
DDR3_WE	IO_L7P_T1_34	AA1
DDR3_ODT	IO_L14N_T2_SRCC_34	U5
DDR3_RESET	IO_L15P_T2_DQS_34	W6
DDR3_CLK_P	IO_L3P_T0_DQS_34	R3
DDR3_CLK_N	IO_L3N_T0_DQS_34	R2
DDR3_CKE	IO_L14P_T2_SRCC_34	T5

5. QSPI Flash

The board is assembled with 128Mbit of QSPI flash memory using an 4-bit data bus. The flash device is N25Q128 which uses 3.3V CMOS signaling standard. Because of its non-volatile property, it is usually used for storing software binaries, images, sounds or other media. Detail information of QSPI FLASH is shown in table 2-5-1 below:

Part	P/N	Capacity	Vender
U8	N25Q128	128M Bit	Numonyx

Table 2-5-1 QSPI Flash Information

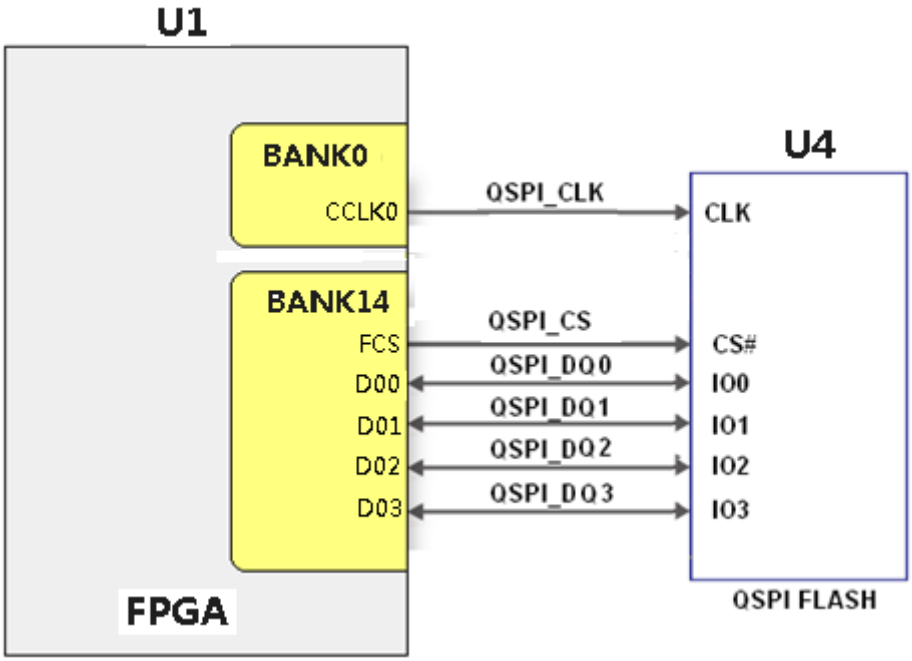


Figure 2-5-1 Connections between FPGA and Flash

Pin Assignment of FLASH：

Net Name	FPGA PIN Name	FPGA P/N
QSPI_CLK	CCLK_0	L12
QSPI_CS	IO_L6P_T0_FCS_B_14	T19
QSPI_DQ0	IO_L1P_T0_D00_MOSI_14	P22
QSPI_DQ1	IO_L1N_T0_D01_DIN_14	R22
QSPI_DQ2	IO_L2P_T0_D02_14	P21
QSPI_DQ3	IO_L2N_T0_D03_14	R21

Figure 2-5-2 shows onboard QSPI FLASH

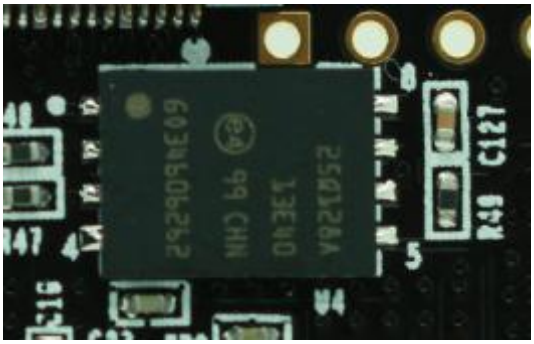


Figure 2-5-2 QSPI FLASH on board

6. LED light

There are three RED LEDs on the FPGA, it includes power indicator LED, done indicator LED and user LED. When the core board is power on, the power indicator LED turns on. When the FPGA configuration is configured, the done LED will be on. The user LED is driven directly by a pin of FPGA, driving its associated pin to a high logic level turns the LED on, and driving the pin low turns it off.

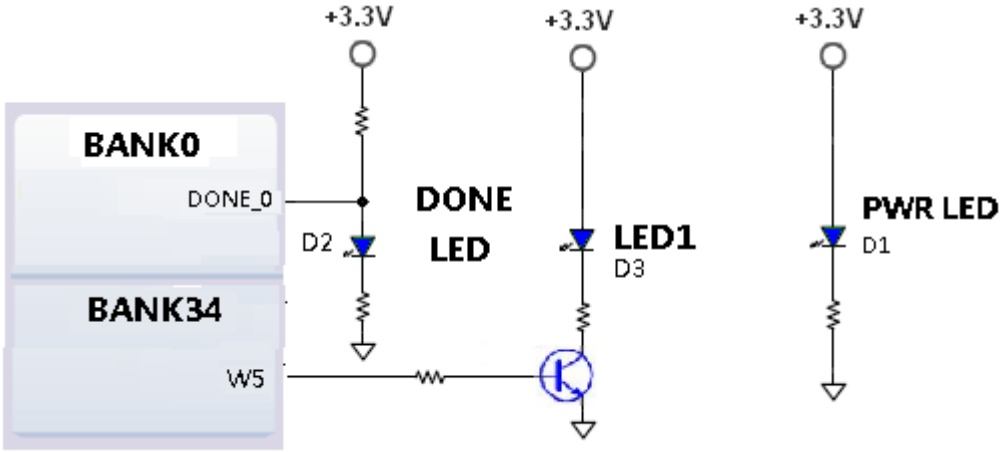


Figure 2-6-1 Connections between the LEDs and FPGA

Figure 2-6-2 is the LEDs on AC7100 board

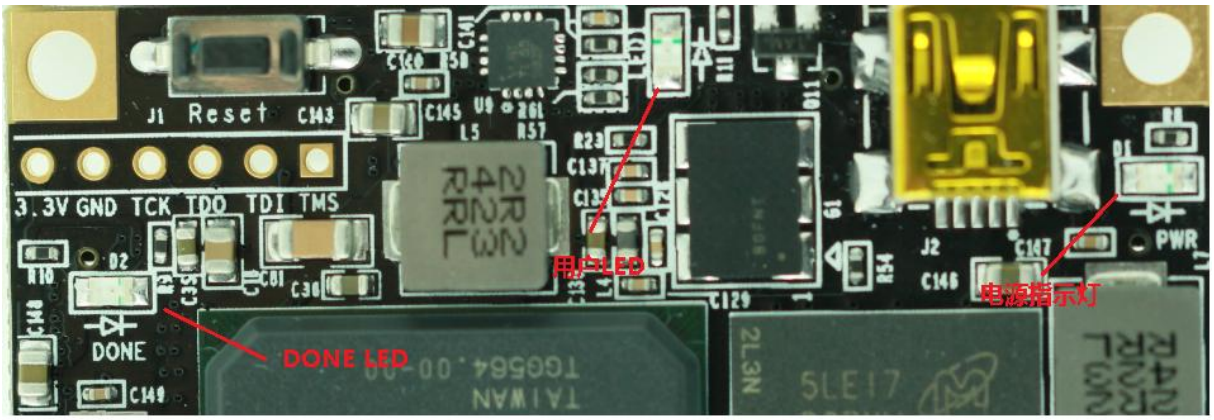


Figure 2-6-2 LEDs on AC7100 board

Pin Assignment of User LED

Net Name	FPGA PIN Name	FPGA P/A	Comments
LED1	IO_L15N_T2_DQS_34	W5	User LED Light

7. Reset Button

AC7100 core board has a reset button, it is connected to the bank34 IO of FPGA. User can use this button to initialize the FPGA program. When reset button is pressed, the reset signal to FPGA is low and the reset is valid. When the button is not pressed, the reset signal is high. The schematic diagram of the reset button connection is shown in Figure 2-7-1

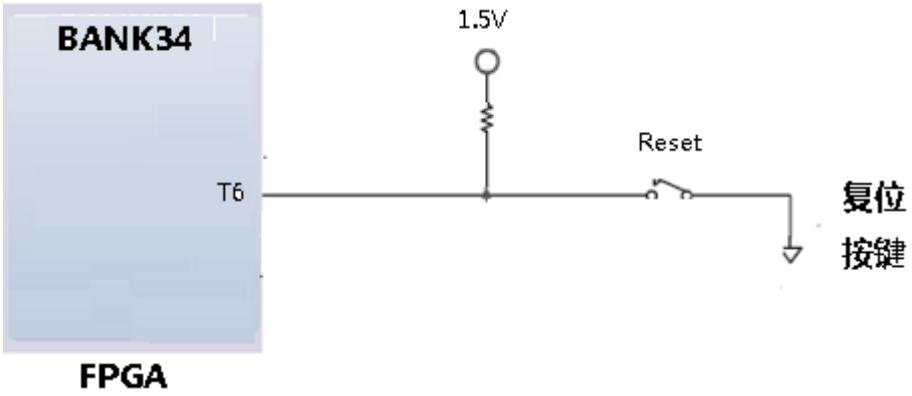


Figure 2-7-1 Connections between the button and FPGA

Figure 2-7-2 is the reset button on AC7100 board

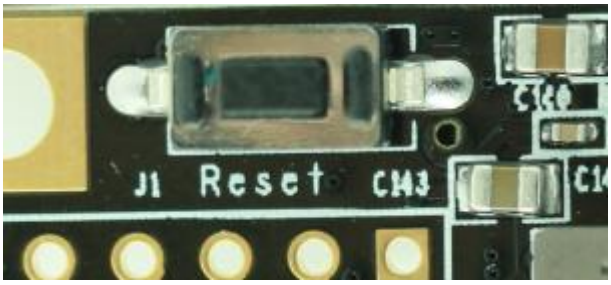


Figure 2-7-2 Reset Button on AC7100 Board

Pin Assignment of Reset Button

Net Name	FPGA PIN Name	FPGA P/N	Comment
RESET_N	IO_L17N_T2_34	T6	Reset Button

8. JTAG Interface

◦ In the AC7100 core board, it reserves a JTAG interface (J1), it is used to download or debug FPGA program without expansion board. Figure 2-8-1 is circuit part of the JTAG port, only four JTAG signals (TMS, TDI, TDO, TCK) are connected to J1 for JTAG access

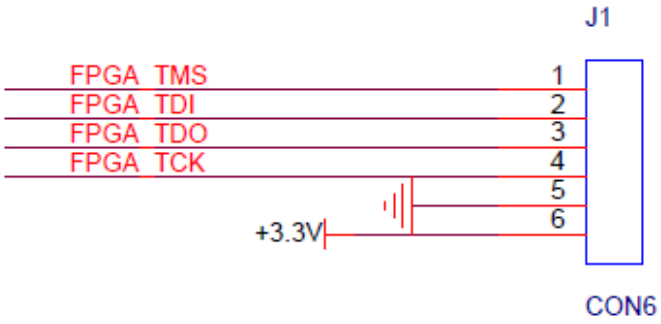


Figure 2-8-1 JTAG interface schematic

In AC7100 core board, the JTAG connector (J1) is not mounted, If user want to use it, please install the JTAG connector with single 6-pins 2.54mm pitch connector. Figure 2-8-2 shows the JTAG connector position on PCB board

Figure 2-8-2 JTAG Interface on board

9. Power Input

In AC7100 core board, we reserved a mini USB port (J2) which can power on core board and work separately without expansion board. Using a USB cable connect to computer, the +5.0V power supply is coming from USB port to power on AC7100 board. Please do not connect other power supply which voltage is higher than +5.0V, it maybe damage the core board. The schematic diagram of the mini USB connection is shown in Figure 2-9-1

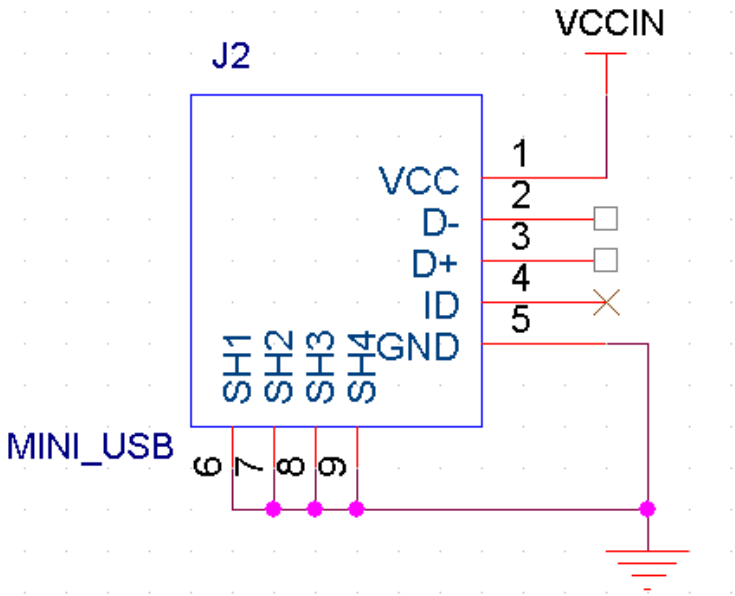


Figure 2-9-1MINI USB Port Schematic

Figure 2-9-2 is mini USB port on AC7100 board

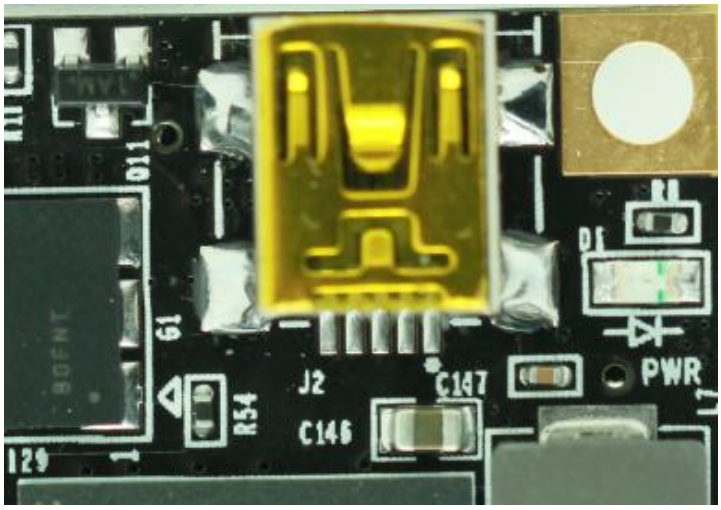


Figure 2-9-2 MINI USB port on AC7100 board

10. Board-to-Board Connector

The core board has four high-speed board-to-board connectors on PCB bottom side. Each connector is 80-pins of 0.5mm pin pitch, which is suitable for high-speed signal transmission. 180 FPGA IOs (include 86 pairs LVDS signals) and all differential signals of GTP transceivers are connected to expansion board through these four connectors.

Connector CON1

CON1 is one of 80-pins connector which is used to connect +5V power signals, ground and FPGA IO signals between core board and expansion board. Please note that the voltage level of IO from FPGA bank34 is +1.5V standard. Table 2-10-1 list

the pin assignment of CON1 connector.

2-10-1 Table： Pin assignment of CN1

CON1 PIN	Net Name	FPGA PIN	Voltage Level	CON1 PIN	Net Name	FPGA PIN	Voltage Level
PIN1	VCCIN	-	+5V	PIN2	VCCIN	-	+5V
PIN3	VCCIN	-	+5V	PIN4	VCCIN	-	+5V
PIN5	VCCIN	-	+5V	PIN6	VCCIN	-	+5V
PIN7	VCCIN	-	+5V	PIN8	VCCIN	-	+5V
PIN9	GND	-	Ground	PIN10	GND	-	地
PIN11	NC	-	-	PIN12	NC	-	-
PIN13	NC	-	-	PIN14	NC	-	-
PIN15	NC	-	-	PIN16	B13_L4_P	AA15	3.3V
PIN17	NC	-	-	PIN18	B13_L4_N	AB15	3.3V
PIN19	GND	-	Ground	PIN20	GND	-	Ground
PIN21	B13_L5_P	Y13	3.3V	PIN22	B13_L1_P	Y16	3.3V
PIN23	B13_L5_N	AA14	3.3V	PIN24	B13_L1_N	AA16	3.3V
PIN25	B13_L7_P	AB11	3.3V	PIN26	B13_L2_P	AB16	3.3V
PIN27	B13_L7_P	AB12	3.3V	PIN28	B13_L2_N	AB17	3.3V
PIN29	GND	-	Ground	PIN30	GND	-	Ground
PIN31	B13_L3_P	AA13	3.3V	PIN32	B13_L6_P	W14	3.3V
PIN33	B13_L3_N	AB13	3.3V	PIN34	B13_L6_N	Y14	3.3V
PIN35	B34_L23_P	Y8	1.5V	PIN36	B34_L20_P	AB7	1.5V
PIN37	B34_L23_N	Y7	1.5V	PIN38	B34_L20_N	AB6	1.5V
PIN39	GND	-	Ground	PIN40	GND	-	Ground
PIN41	B34_L18_N	AA6	1.5V	PIN42	B34_L21_N	V8	1.5V
PIN43	B34_L18_P	Y6	1.5V	PIN44	B34_L21_P	V9	1.5V
PIN45	B34_L19_P	V7	1.5V	PIN46	B34_L22_P	AA8	1.5V
PIN47	B34_L19_N	W7	1.5V	PIN48	B34_L22_N	AB8	1.5V
PIN49	GND	-	Ground	PIN50	GND	-	Ground
PIN51	XADC_VN	M9	ADC	PIN52	NC		
PIN53	XADC_VP	L10	ADC	PIN54	B34_L25	U7	1.5V
PIN55	NC	-	-	PIN56	B34_L24_P	W9	1.5V
PIN57	NC	-	-	PIN58	B34_L24_N	Y9	1.5V
PIN59	GND	-	Ground	PIN60	GND	-	Ground
PIN61	B16_L1_N	F14	3.3V	PIN62	NC	-	-
PIN63	B16_L1_P	F13	3.3V	PIN64	NC	-	-
PIN65	B16_L4_N	E14	3.3V	PIN66	NC	-	-
PIN67	B16_L4_P	E13	3.3V	PIN68	NC	-	-
PIN69	GND	-	Ground	PIN70	GND	-	Ground
PIN71	B16_L6_N	D15	3.3V	PIN72	NC	-	-

PIN73	B16_L6_P	D14	3.3V	PIN74	NC	-	-
PIN75	B16_L8_P	C13	3.3V	PIN76	NC	-	-
PIN77	B16_L8_N	B13	3.3V	PIN78	NC	-	-
PIN79	NC	-	-	PIN80	NC	-	-

Figure 2-10-1 is the CON1 connector on core board, and the pin1 of connector is marked on the board.

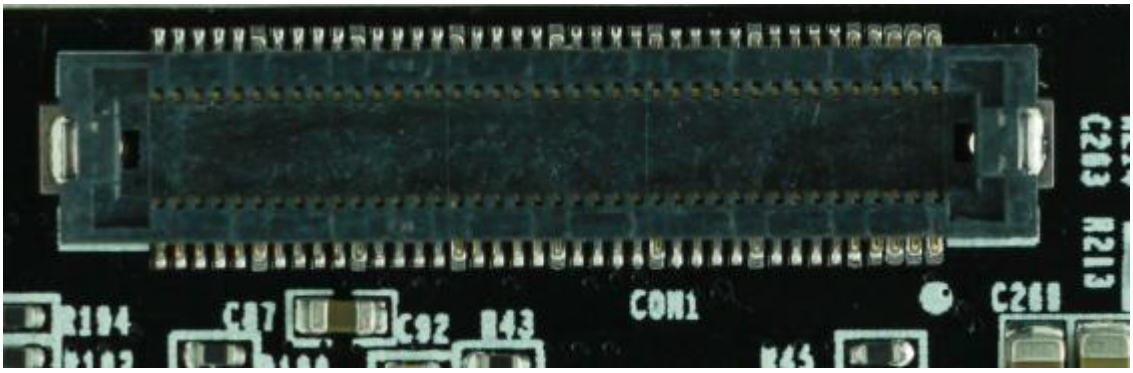


Figure 2-10-1 CON Connector on board

CON2 Connector

The 80-Pin connector CON2 is used to extend the IOs of FPGA bank13 and bank14, the voltage level of these IOs are +3.3V standard. The pin assignment of the CON2 connector is shown in table 2-10-2：

Table 2-10-2: Pin Assignment of CON2

CON2 PIN	Net Name	FPGA PIN	Voltage Standard	CON2 PIN	Net Name	FPGA PIN	Voltage Standard
PIN1	B13_L16_P	W15	3.3V	PIN2	B14_L16_P	V17	3.3V
PIN3	B13_L16_N	W16	3.3V	PIN4	B14_L16_N	W17	3.3V
PIN5	B13_L15_P	T14	3.3V	PIN6	B13_L14_P	U15	3.3V
PIN7	B13_L15_N	T15	3.3V	PIN8	B13_L14_N	V15	3.3V
PIN9	GND	-	Ground	PIN10	GND	-	Ground
PIN11	B13_L13_P	V13	3.3V	PIN12	B14_L10_P	AB21	3.3V
PIN13	B13_L13_N	V14	3.3V	PIN14	B14_L10_N	AB22	3.3V
PIN15	B13_L12_P	W11	3.3V	PIN16	B14_L8_N	AA21	3.3V
PIN17	B13_L12_N	W12	3.3V	PIN18	B14_L8_P	AA20	3.3V
PIN19	GND	-	Ground	PIN20	GND	-	Ground
PIN21	B13_L11_P	Y11	3.3V	PIN22	B14_L15_N	AB20	3.3V
PIN23	B13_L11_N	Y12	3.3V	PIN24	B14_L15_P	AA19	3.3V
PIN25	B13_L10_P	V10	3.3V	PIN26	B14_L17_P	AA18	3.3V
PIN27	B13_L10_N	W10	3.3V	PIN28	B14_L17_N	AB18	3.3V
PIN29	GND	-	Ground	PIN30	GND	-	Ground
PIN31	B13_L9_N	AA11	3.3V	PIN32	B14_L6_N	T20	3.3V
PIN33	B13_L9_P	AA10	3.3V	PIN34	B13_IO0	Y17	3.3V
PIN35	B13_L8_N	AB10	3.3V	PIN36	B14_L7_N	W22	3.3V

PIN37	B13_L8_P	AA9	3.3V	PIN38	B14_L7_P	W21	3.3V
PIN39	GND	-	Ground	PIN40	GND	-	Ground
PIN41	B14_L11_N	V20	3.3V	PIN42	B14_L4_P	T21	3.3V
PIN43	B14_L11_P	U20	3.3V	PIN44	B14_L4_N	U21	3.3V
PIN45	B14_L14_N	V19	3.3V	PIN46	B14_L9_P	Y21	3.3V
PIN47	B14_L14_P	V18	3.3V	PIN48	B14_L9_N	Y22	3.3V
PIN49	GND	-	Ground	PIN50	GND	-	Ground
PIN51	B14_L5_N	R19	3.3V	PIN52	B14_L12_N	W20	3.3V
PIN53	B14_L5_P	P19	3.3V	PIN54	B14_L12_P	W19	3.3V
PIN55	B14_L18_N	U18	3.3V	PIN56	B14_L13_N	Y19	3.3V
PIN57	B14_L18_P	U17	3.3V	PIN58	B14_L13_P	Y18	3.3V
PIN59	GND	-	Ground	PIN60	GND	-	Ground
PIN61	B13_L17_P	T16	3.3V	PIN62	B14_L3_N	V22	3.3V
PIN63	B13_L17_N	U16	3.3V	PIN64	B14_L3_P	U22	3.3V
PIN65	B14_L21_N	P17	3.3V	PIN66	B14_L20_N	T18	3.3V
PIN67	B14_L21_P	N17	3.3V	PIN68	B14_L20_P	R18	3.3V
PIN69	GND	-	Ground	PIN70	GND	-	Ground
PIN71	B14_L22_P	P15	3.3V	PIN72	B14_L19_N	R14	3.3V
PIN73	B14_L22_N	R16	3.3V	PIN74	B14_L19_P	P14	3.3V
PIN75	B14_L24_N	R17	3.3V	PIN76	B14_L23_P	N13	3.3V
PIN77	B14_L24_P	P16	3.3V	PIN78	B14_L23_N	N14	3.3V
PIN79	B14_IO0	P20	3.3V	PIN80	B14_IO25	N15	3.3V

Figure 2-10-2 is the CON2 connector on core board, and the pin1 of connector is marked on the board.

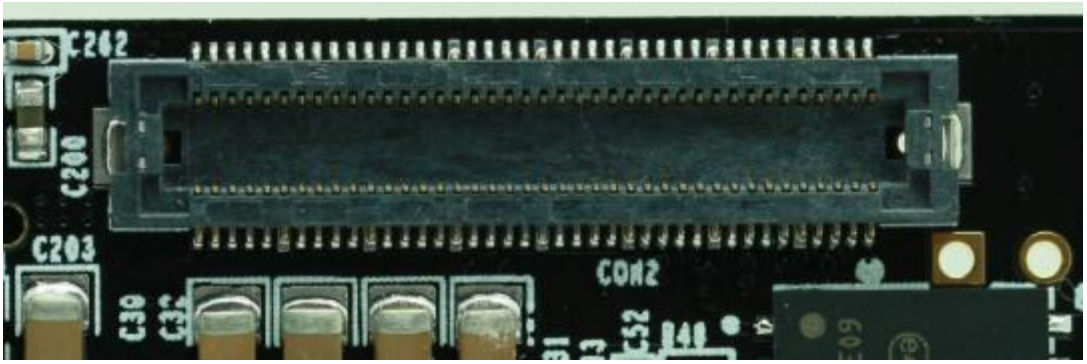


Figure 2-10-2 CON2 Connector Onboard

Connector CON3

The 80-Pin connector CON3 is used to extend the IOs of FPGA bank15 and bank16, the voltage level of these IOs are +3.3V standard by default, but it can be changed to other voltage level if we change the VCCO power supply of bank15 and bank16 by replacing the LDO chipset. Three JTAG signals also connected to CON3 connector for expansion board to access the JTAG interface. The pin assignment of the CON3 connector is shown in table 2-10-3.

2-10-3 Table： Pin Assignment of CON3 Connector

CON3 PIN	Net Name	FPGA PIN	Voltage Level	CON3 PIN	Net Name	FPGA PIN	Voltage Level
PIN1	B15_IO0	J16	3.3V	PIN2	B15_IO25	M17	3.3V
PIN3	B16_IO0	F15	3.3V	PIN4	B16_IO25	F21	3.3V
PIN5	B15_L4_P	G17	3.3V	PIN6	B16_L21_N	A21	3.3V
PIN7	B15_L4_N	G18	3.3V	PIN8	B16_L21_P	B21	3.3V
PIN9	GND	-	Ground	PIN10	GND	-	Ground
PIN11	B15_L2_P	G15	3.3V	PIN12	B16_L23_P	E21	3.3V
PIN13	B15_L2_N	G16	3.3V	PIN14	B16_L23_N	D21	3.3V
PIN15	B15_L12_P	J19	3.3V	PIN16	B16_L22_P	E22	3.3V
PIN17	B15_L12_N	H19	3.3V	PIN18	B16_L22_N	D22	3.3V
PIN19	GND	-	Ground	PIN20	GND	-	Ground
PIN21	B15_L11_P	J20	3.3V	PIN22	B16_L24_P	G21	3.3V
PIN23	B15_L11_N	J21	3.3V	PIN24	B16_L24_N	G22	3.3V
PIN25	B15_L1_N	G13	3.3V	PIN26	B15_L8_N	G20	3.3V
PIN27	B15_L1_P	H13	3.3V	PIN28	B15_L8_P	H20	3.3V
PIN29	GND	-	Ground	PIN30	GND	-	Ground
PIN31	B15_L5_P	J15	3.3V	PIN32	B15_L7_N	H22	3.3V
PIN33	B15_L5_N	H15	3.3V	PIN34	B15_L7_P	J22	3.3V
PIN35	B15_L3_N	H14	3.3V	PIN36	B15_L9_P	K21	3.3V
PIN37	B15_L3_P	J14	3.3V	PIN38	B15_L9_N	K22	3.3V
PIN39	GND	-	Ground	PIN40	GND	-	Ground
PIN41	B15_L19_P	K13	3.3V	PIN42	B15_L15_N	M22	3.3V
PIN43	B15_L19_N	K14	3.3V	PIN44	B15_L15_P	N22	3.3V
PIN45	B15_L20_P	M13	3.3V	PIN46	B15_L6_N	H18	3.3V
PIN47	B15_L20_N	L13	3.3V	PIN48	B15_L6_P	H17	3.3V
PIN49	GND	-	Ground	PIN50	GND	-	Ground
PIN51	B15_L14_P	L19	3.3V	PIN52	B15_L13_N	K19	3.3V
PIN53	B15_L14_N	L20	3.3V	PIN54	B15_L13_P	K18	3.3V
PIN55	B15_L21_P	K17	3.3V	PIN56	B15_L10_P	M21	3.3V
PIN57	B15_L21_N	J17	3.3V	PIN58	B15_L10_N	L21	3.3V
PIN59	GND	-	Ground	PIN60	GND	-	Ground
PIN61	B15_L23_P	L16	3.3V	PIN62	B15_L18_P	N20	3.3V
PIN63	B15_L23_N	K16	3.3V	PIN64	B15_L18_N	M20	3.3V
PIN65	B15_L22_P	L14	3.3V	PIN66	B15_L17_N	N19	3.3V
PIN67	B15_L22_N	L15	3.3V	PIN68	B15_L17_P	N18	3.3V
PIN69	GND	-	Ground	PIN70	GND	-	Ground
PIN71	B15_L24_P	M15	3.3V	PIN72	B15_L16_P	M18	3.3V
PIN73	B15_L24_N	M16	3.3V	PIN74	B15_L16_N	L18	3.3V
PIN75	NC	-		PIN76	NC	-	

PIN77	FPGA_TCK	V12	3.3V	PIN78	FPGA_TDI	R13	3.3V
PIN79	FPGA_TDO	U13	3.3V	PIN80	FPGA_TMS	T13	3.3V

Figure 2-10-3 is the CON3 connector on core board, and the pin1 of connector is marked on the board.

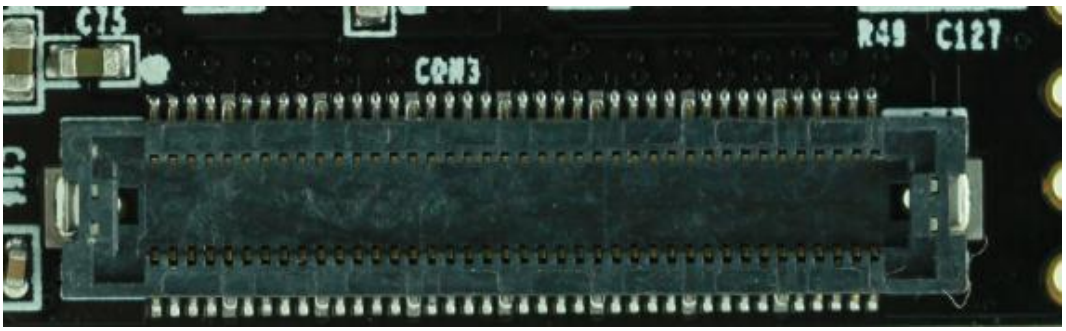


Figure 2-10-3 CON3 Connector on board

Connector CON4

The 80-Pin connector CON4 is used to extend the IOs of FPGA bank16, high speed data of GTP transceivers and clock signals. The voltage level of these IOs is +3.3V standard by default, but it can be changed to other voltage level if we change the VCCO power supply of Bank16 by replacing the LDO chipset. High speed data lines of GTP and clock signals on core board, are equals in length and maintain in a certain intervals, could prevent signal interference

Table 2-10-4：Pin Assignment of CON4

CON4 PIN	Net Name	FPGA PIN	Voltage Level	CON4 PIN	Net Name	FPGA PIN	Voltage Level
PIN1	NC		-	NC		-	NC
PIN3	NC		-	NC		-	NC
PIN5	NC		-	NC		-	NC
PIN7	NC		-	NC		-	NC
PIN9	GND	-	Ground	PIN10	GND	-	Ground
PIN11	NC		-	PIN12	MGT_TX2_P	B6	Difference
PIN13	NC		-	PIN14	MGT_TX2_N	A6	Difference
PIN15	GND	-	GND	PIN16	GND	-	Ground
PIN17	MGT_TX3_P	D7	Difference	PIN18	MGT_RX2_P	B10	Difference
PIN19	MGT_TX3_N	C7	Difference	PIN20	MGT_RX2_N	A10	Difference
PIN21	GND	-	Ground	PIN22	GND	-	Ground
PIN23	MGT_RX3_P	D9	Difference	PIN24	MGT_TX0_P	B4	Difference
PIN25	MGT_RX3_N	C9	Difference	PIN26	MGT_TX0_N	A4	Difference
PIN27	GND	-	Ground	PIN28	GND	-	Ground
PIN29	MGT_TX1_P	D5	Difference	PIN30	MGT_RX0_P	B8	Difference
PIN31	MGT_TX1_N	C5	Difference	PIN32	MGT_RX0_N	A8	Difference
PIN33	GND	-	Ground	PIN34	GND	-	Ground
PIN35	MGT_RX1_P	D11	Difference	PIN36	MGT_CLK1_P	F10	Difference
PIN37	MGT_RX1_N	C11	Difference	PIN38	MGT_CLK1_N	E10	Difference
PIN39	GND	-	Ground	PIN40	GND	-	Ground
PIN41	B16_L5_P	E16	3.3V	PIN42	B16_L2_P	F16	3.3V
PIN43	B16_L5_N	D16	3.3V	PIN44	B16_L2_N	E17	3.3V
PIN45	B16_L7_P	B15	3.3V	PIN46	B16_L3_P	C14	3.3V
PIN47	B16_L7_N	B16	3.3V	PIN48	B16_L3_N	C15	3.3V
PIN49	GND	-	Ground	PIN50	GND	-	Ground
PIN51	B16_L9_P	A15	3.3V	PIN52	B16_L10_P	A13	3.3V
PIN53	B16_L9_N	A16	3.3V	PIN54	B16_L10_N	A14	3.3V
PIN55	B16_L11_P	B17	3.3V	PIN56	B16_L12_P	D17	3.3V
PIN57	B16_L11_N	B18	3.3V	PIN58	B16_L12_N	C17	3.3V
PIN59	GND	-	Ground	PIN60	GND	-	Ground
PIN61	B16_L13_P	C18	3.3V	PIN62	B16_L14_P	E19	3.3V
PIN63	B16_L13_N	C19	3.3V	PIN64	B16_L14_N	D19	3.3V
PIN65	B16_L15_P	F18	3.3V	PIN66	B16_L16_P	B20	3.3V
PIN67	B16_L15_N	E18	3.3V	PIN68	B16_L16_N	A20	3.3V
PIN69	GND	-	Ground	PIN70	GND	-	Ground
PIN71	B16_L17_P	A18	3.3V	PIN72	B16_L18_P	F19	3.3V
PIN73	B16_L17_N	A19	3.3V	PIN74	B16_L18_N	F20	3.3V

PIN75	B16_L19_P	D20	3.3V	PIN76	B16_L20_P	C22	3.3V
PIN77	B16_L19_N	C20	3.3V	PIN78	B16_L20_N	B22	3.3V
PIN79	NC	-		PIN80	NC	-	

Figure 2-10-4 is the CON4 connector on core board, and the pin1 of connector is marked on the board.

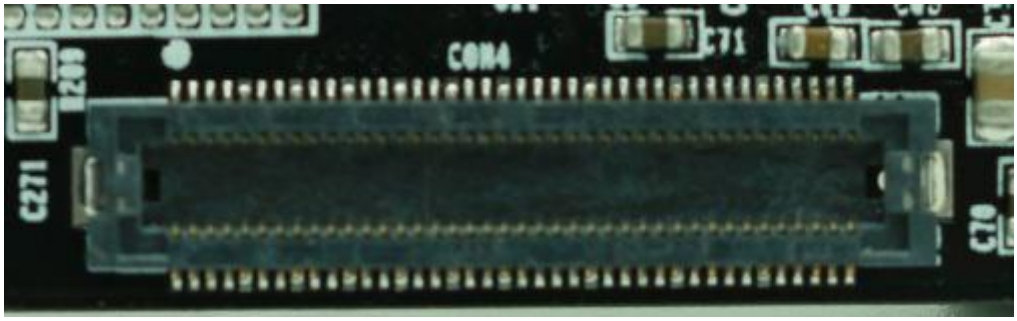


Figure 2-10-4 CON4 Connector on board

11. Power

The power supply voltage of the AC7100 core board is DC5V and can supply from mini USB port or board-to-board connector from expansion board. Please note that the mini USB and expansion board cannot supply power to core board at the same time, it maybe damage the USB port of computer. The schematic diagram of the power supply on the board is shown in figure 2-11-1 below.

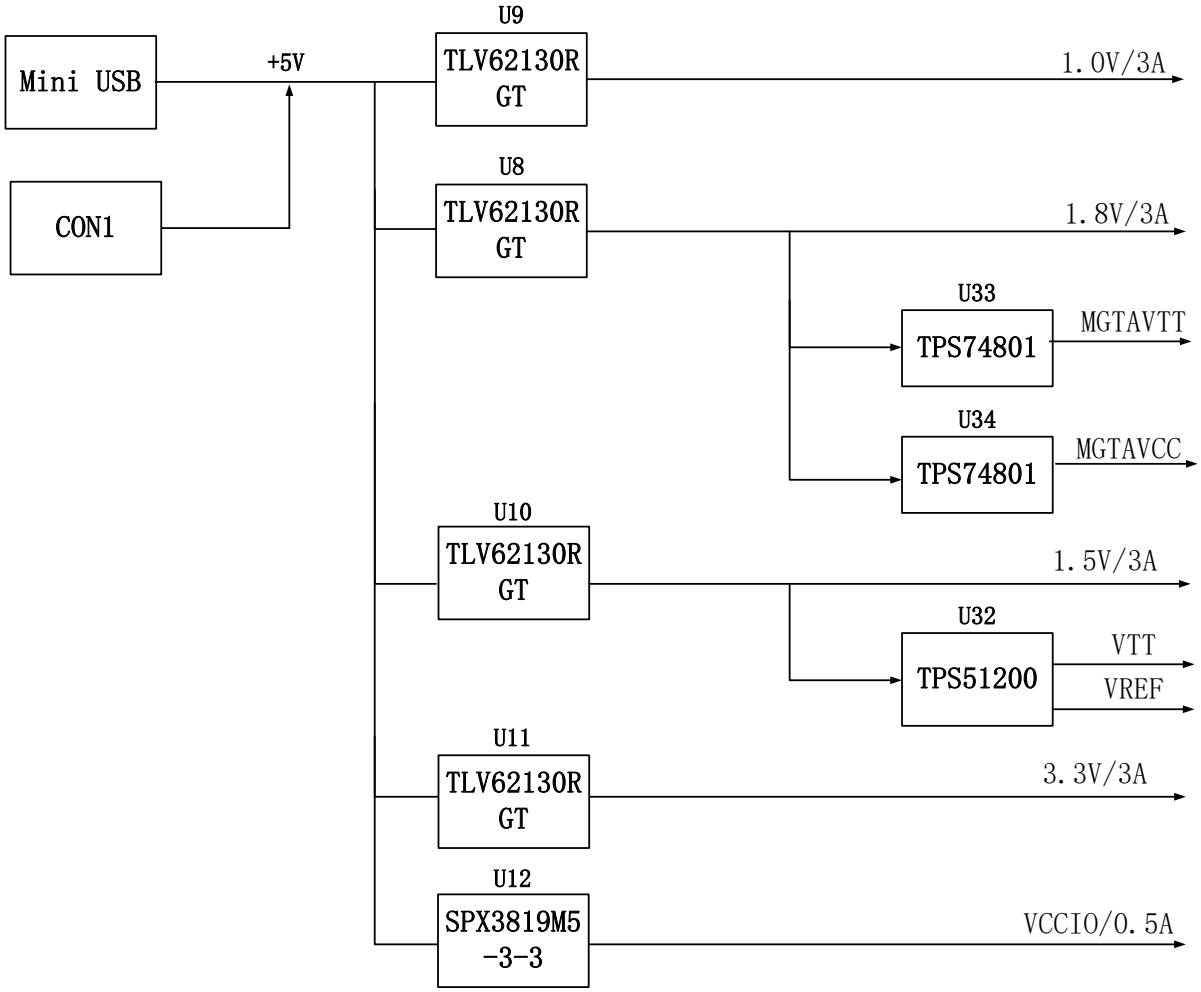


Figure2-11-1 Power design

AC7100 core board uses the +5V power to generate +3.3V, +1.5V, +1.8V and +1.0V power output through the DC/DC power convertor. The output current of each power can be as high as 3A. AC7100 core board uses a LDO chipset of SPX3819M5-3-3 to generate +3.3V power supply for VCCIO power of FPGA bank15 and bank16. it is easy for use to change the voltage standard of IOs by replacing of the LDO chipset. The +1.5V power generates the required VTT and VREF voltages for DDR3 through the TI TPS51200 chipset. And+1.8V power generates the MGTAVTT and MGTAVCC power of GTP transceiver through the TI LDO chipset (TPS74801).

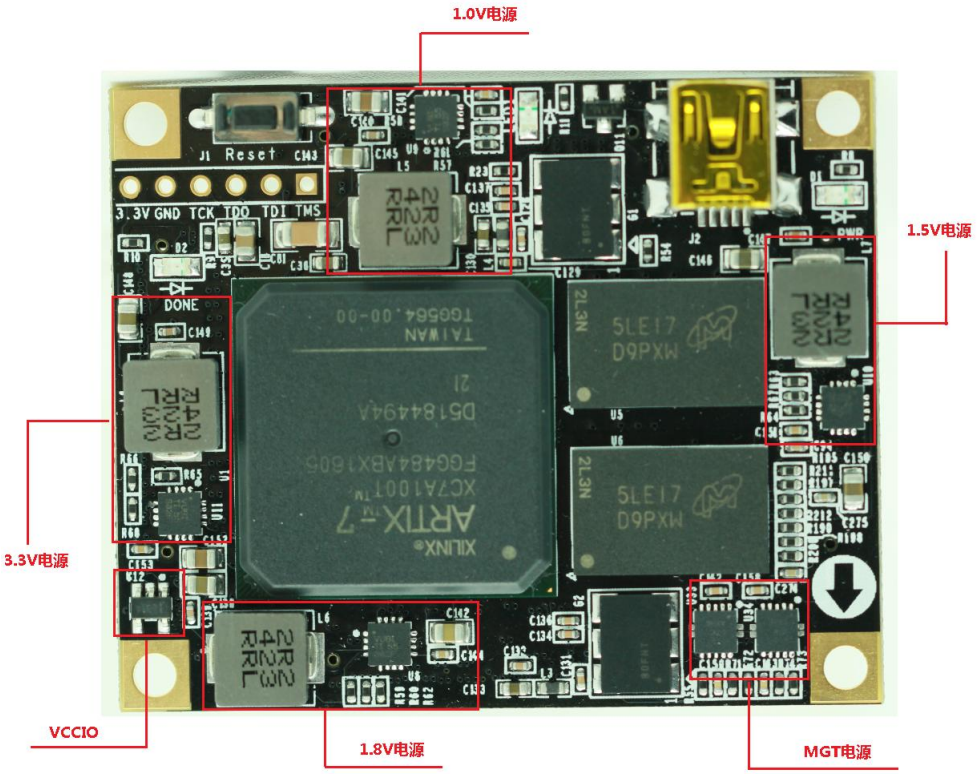
The functions of each power distribution are shown below:

Power	Distribution
+3.3V	FPGA Bank0,Bank13，Bank14 的 VCCIO, QSIP FLASH, Clock Oscillators
+1.8V	FPGA auxiliary Power, TPS74801 Power supply
+1.0V	FPGA Core power
+1.5V	DDR3, FPGA Bank34 and Bank35
VREF, VTT（+0.75V）	DDR3
VCCIO(+3.3V)	FPGA Bank15, Bank16
MGTAVTT(+1.2V)	FPGA GTP Transceivers, Bank216

MGTAVCC(+1.0V)	FPGA GTP Transceivers, Bank216

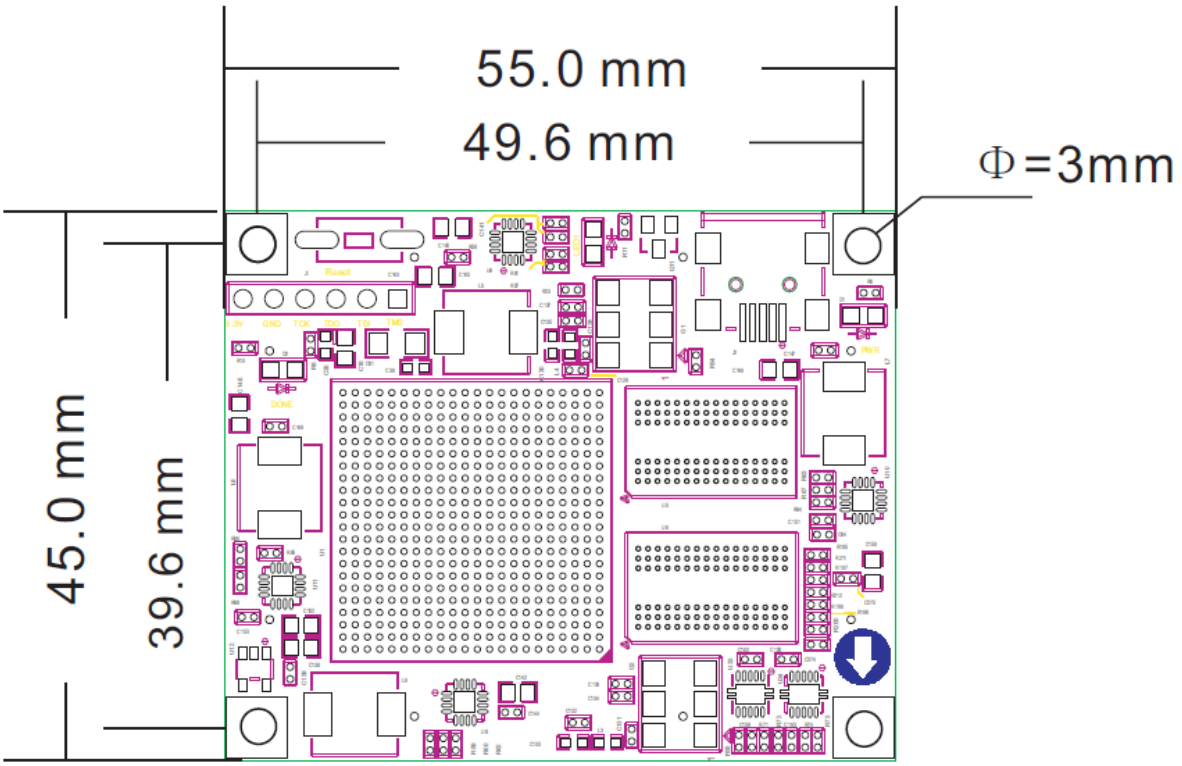
There is requirement of power supply sequencing of Artix-7 FPGA, AC7100 core board is designed to meet it, the orders of power on for each power supply is as following: +1.0V -> +1.8V -> +1.5 V, +3.3V, VCCIO

Power circuit on AC7100 core board is showed in Figure 2-11-2 below.

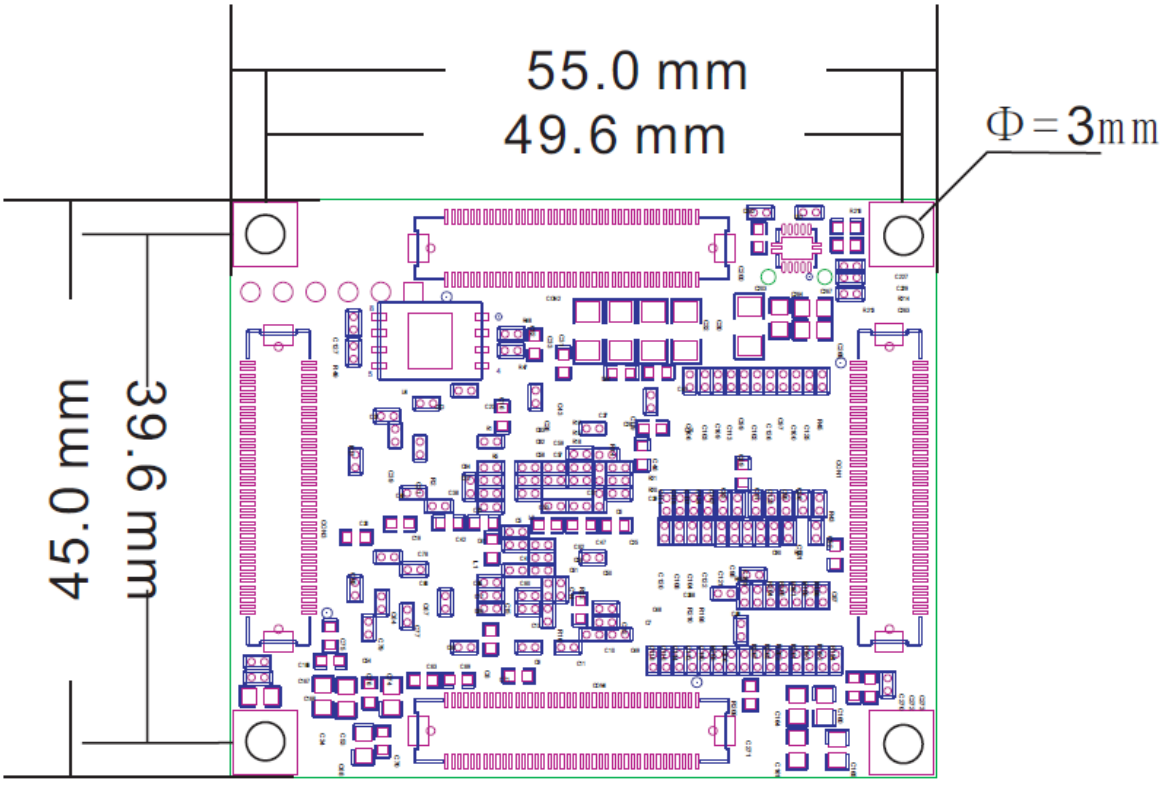


2-11-2 Power of AC7100 on core board

12. Mechanical



Top View



Bottom View

Expansion Board

1. Preview

The following features are provided on the AX7102 expansion board:

- 1-channel PCIe x4 high speed data transmission Connector
- 2-channels 10/100M/1000M Ethernet RJ-45 Connector
- 1-channel HDMI Video Input Connector
- 1-channel HDMI Video Ouput Connector
- 1-channel USB Uart Communication Interface
- SD card Connector
- XADC Connector
- EEPROM with IIC interface
- 2-channels 40-pin IO Headers
- JTAG Debug Connectors
- 2 User Buttons
- 4 User LEDs

2. Gigabit Ethernet

The AX7103 development board provided network communication service to user by two KSZ9031RNX Ethernet PHY chips of Micrel company. The Ethernet PHY chips connected to IOs connectors of ARTIX7 FPGA. The KSZ9031RNX chips supported 10/100/1000 Mbps network transfer transmission rate, by data communication between RGMII connector and FPGA. The KSZ9031RNX supported MDI/MDX and Master/Slave various speed adaptation, Supported MDIO Bus PHY register management.

KSZ9031RNX will detect some specific IO level when power-on, so as to determine the operation mode. The table 3-2-1 described the default setting in AX7103 board after the GPHY chip is power-on.

Configure Pin	Description	Value
PHYAD[2:0]	PHY Address on MDIO/MDC Mode	PHY Address 011
CLK125_EN	Enable of 125Mhz clock	Enable
LED_MODE	LED Mode configure	Single LED Mode
MODE0~MODE3	Link adaptation and full duplex configuration	10/100/1000 adaptation, Compatible with full duplex, half duplex

Table 3-2-1 PHY Chip Default Configuration

When network connected to Gigabit Ethernet, data transmission between FPGA and PHY chip KSZ9031RNX by RGMII bus communication, transfer clock is 125Mhz, the data is sampled on the rising edged and the falling edged of clock.

Figure 3-2-1 showed the connections between the FPGA, 2 Gigabit Ethernet PHY chips

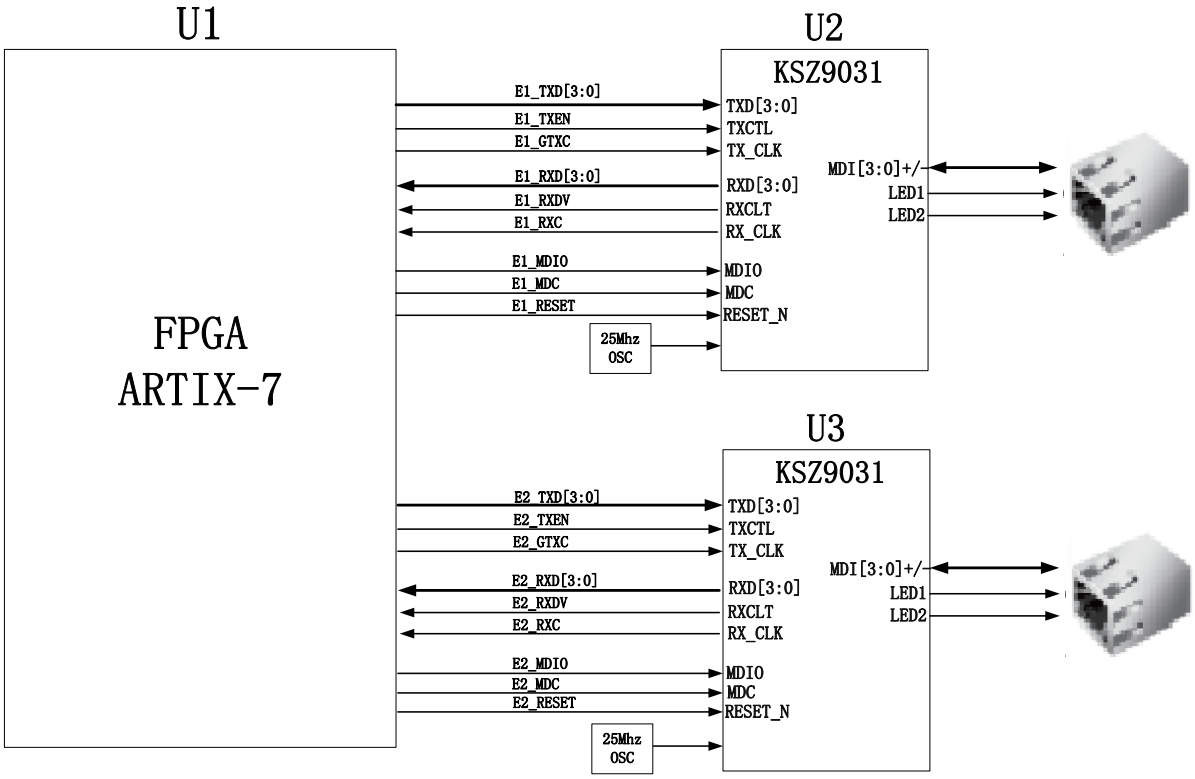


Figure 3-2-1 FPGA and PHY chips connection diagram

Figure 3-2-2is the Ethernet PHY chips on board

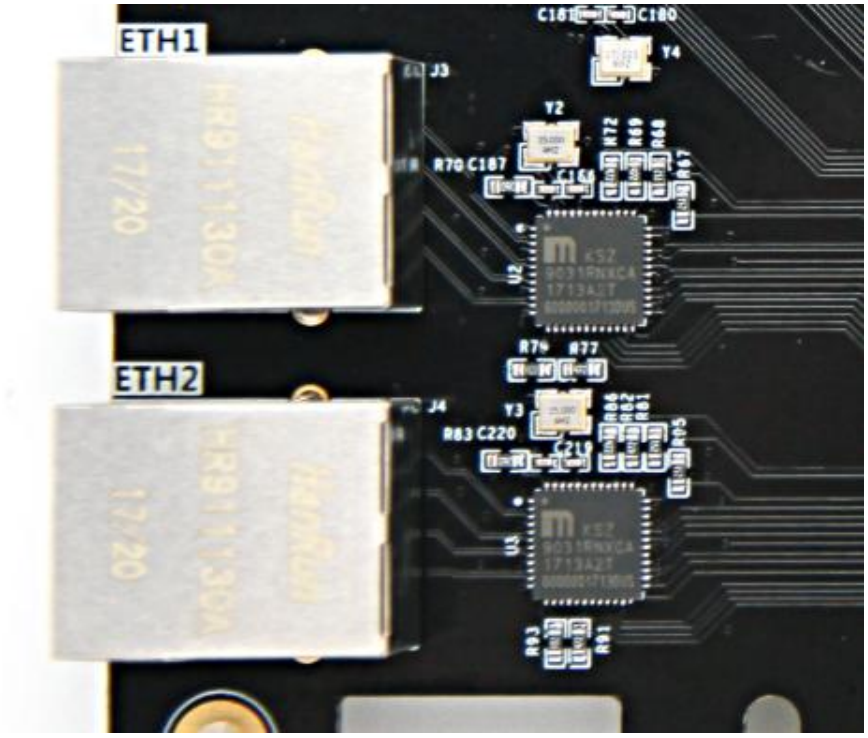


Figure 3-2-2 Ethernet PHY chips on board

The FPGA pins assignment to PHY1 as below:

Net name	FPGA Pin	Comments
E1_GTXC	E18	RGMII Transmit Clock
E1_TXD0	C20	RGMII Transmit Data bit 0
E1_TXD1	D20	RGMII Transmit Data bit1
E1_TXD2	A19	RGMII Transmit Data bit2
E1_TXD3	A18	RGMII Transmit Data bit3
E1_TXEN	F18	RGMII Transmit Enable
E1_RXC	B17	RGMII Receive Clock
E1_RXD0	A16	RGMII Receive Data Bit0
E1_RXD1	B18	RGMII Receive Data Bit1
E1_RXD2	C18	RGMII Receive Data Bit2
E1_RXD3	C19	RGMII Receive Data Bit3
E1_RXDV	A15	RGMII Receive Data Enable
E1_MDC	B16	MDIO Management Clock
E1_MDIO	B15	MDIO Management Data
E1_RESET	D16	PHY chip reset

The FPGA pins assignment to PHY2 as below:

Net name	FPGA Pin	Comments
E2_GTXC	A14	RGMII Transmit Clock
E2_TXD0	E17	RGMII Transmit Data bit 0
E2_TXD1	C14	RGMII Transmit Data bit1
E2_TXD2	C15	RGMII Transmit Data bit2
E2_TXD3	A13	RGMII Transmit Data bit3
E2_TXEN	D17	RGMII Transmit Enable
E2_RXC	E19	RGMII Receive Clock
E2_RXD0	A20	RGMII Receive Data Bit0
E2_RXD1	B20	RGMII Receive Data Bit1
E2_RXD2	D19	RGMII Receive Data Bit2
E2_RXD3	C17	RGMII Receive Data Bit3
E2_RXDV	F19	RGMII Receive Data Enable
E2_MDC	F20	MDIO Management Clock
E2_MDIO	C22	MDIO Management Data
E2_RESET	B22	PHY chip reset

3. PCIe x4 Connector

The AX7103 expansion board provide one industrial level high-speed data transmission PCIe x4, the PICE dimension comply with standard PICE card electrical specification, could use directly on the x4 PCIe slots of PC.

The Transmit/ Receive signal of PCIe connectors connected to GTP transceiver of FPGA. 4 channels of TX signals and RX signals all connected to FPGA by differential signal methods. Single channel communication rate up to 5G bit bandwith. The reference clock of FPGA PCIe provided by PCIe slots of PC, the reference clock is 100Mhz。

The design schematic of FPGA PCIe connector, refer to below figure 3-3-1, the Transmit/ Receive signal and reference clock CLK connected by AC coupled mode.

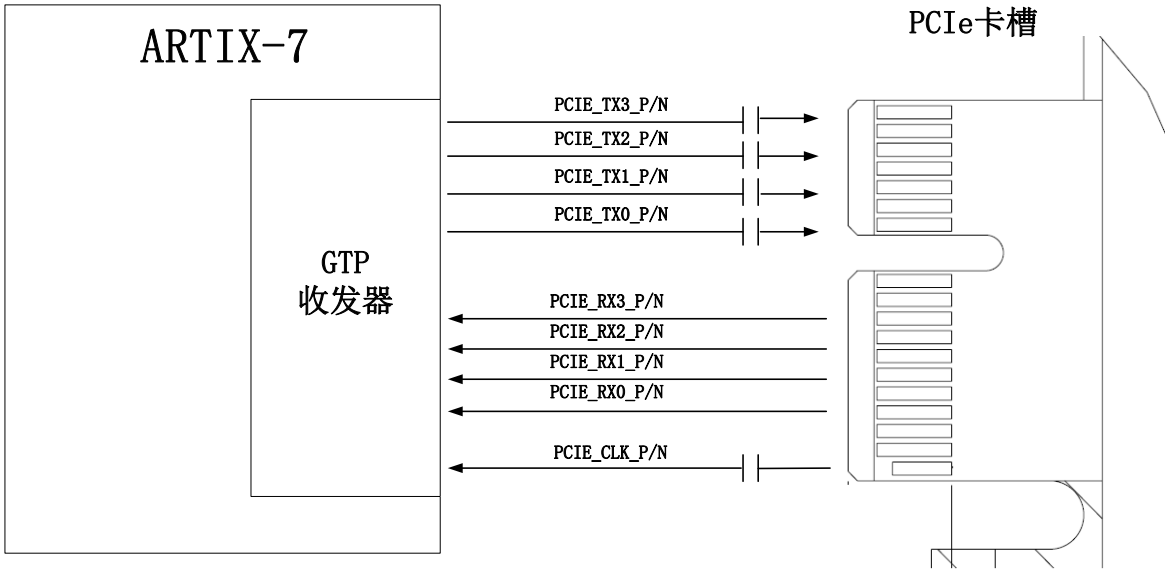
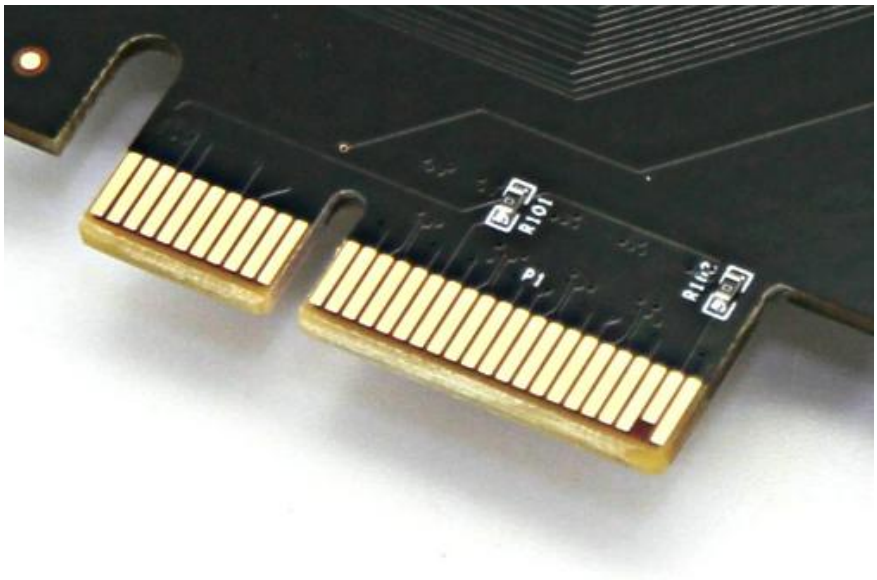


Figure 3-3-1 PCIe x4 Design Schematic

PCIex4 connectors on board, picture as below:



PCIe x4 connectors on board

The FPGA Pins assignment to PCIe x4 connectors

Network Name	FPGA Pins	Comments
PCIE_RX0_P	D11	PCIE channel 0 data receiver Positive
PCIE_RX0_N	C11	PCIE channel 0 data receiver Positive

		Negative
PCIE_RX1_P	B8	PCIE channel 1 data receiver Positive
PCIE_RX1_N	A8	PCIE channel 1 data receiver Negative
PCIE_RX2_P	B10	PCIE channel 2 data receiver Positive
PCIE_RX2_N	A10	PCIE channel 2 data receiver Negative
PCIE_RX3_P	D9	PCIE channel 3 data receiver Positive
PCIE_RX3_N	C9	PCIE channel 3 data receiver Negative
PCIE_TX0_P	D5	PCIE channel 0 data Transmit Positive
PCIE_TX0_N	C5	PCIE channel 0 data Transmit Negative
PCIE_TX1_P	B4	PCIE channel 1 data Transmit Positive
PCIE_TX1_N	A4	PCIE channel 1 data Transmit Negative
PCIE_TX2_P	B6	PCIE channel 2 data Transmit Positive
PCIE_TX2_N	A6	PCIE channel 2 data Transmit Negative
PCIE_TX3_P	D7	PCIE channel 3 data Transmit Positive
PCIE_TX3_N	C7	PCIE channel 3 data Transmit Negative
PCIE_CLK_P	F10	PCIE Reference Clock Positive
PCIE_CLK_N	E10	PCIE Reference Clock Negative

4. HDMI Input Connector

HDMI Output connector, Used the code chips SIL9134 HDMI（DVI） of Silion Image company, supported output up to 1080P@60Hz, supported 3D output. The IIC configure connectors of SIL9134 connected to IOs FPGA. To initialized and controlled the SIL9134 by FPGA program. HDMI output connectors hardware designation as Figure 3-4-1:

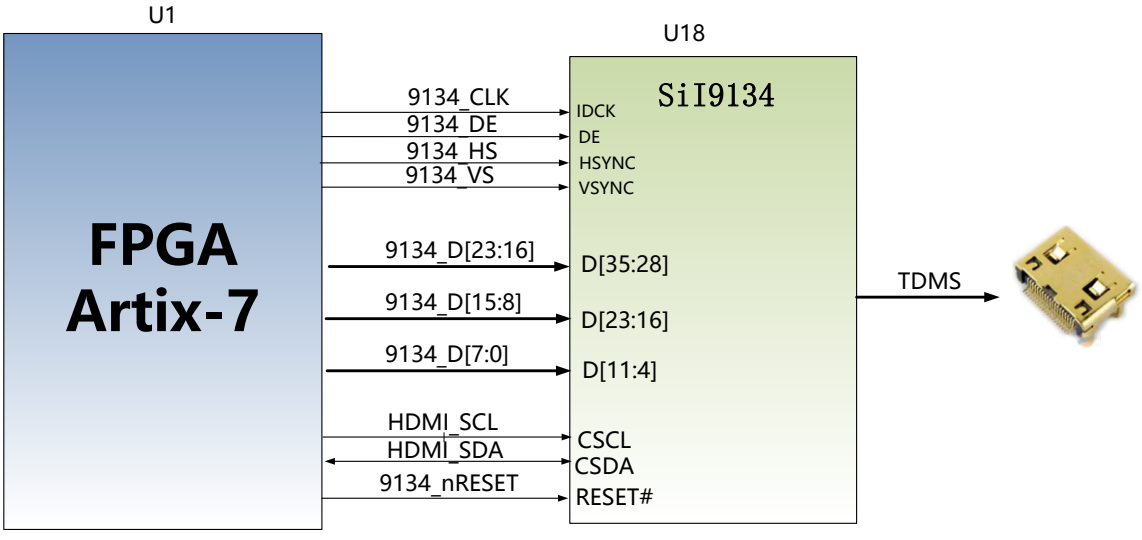


图3-4-1 HDMI Output connector schematic

HDMI Output Connector on board, the pictures as below Figure 3-4-2

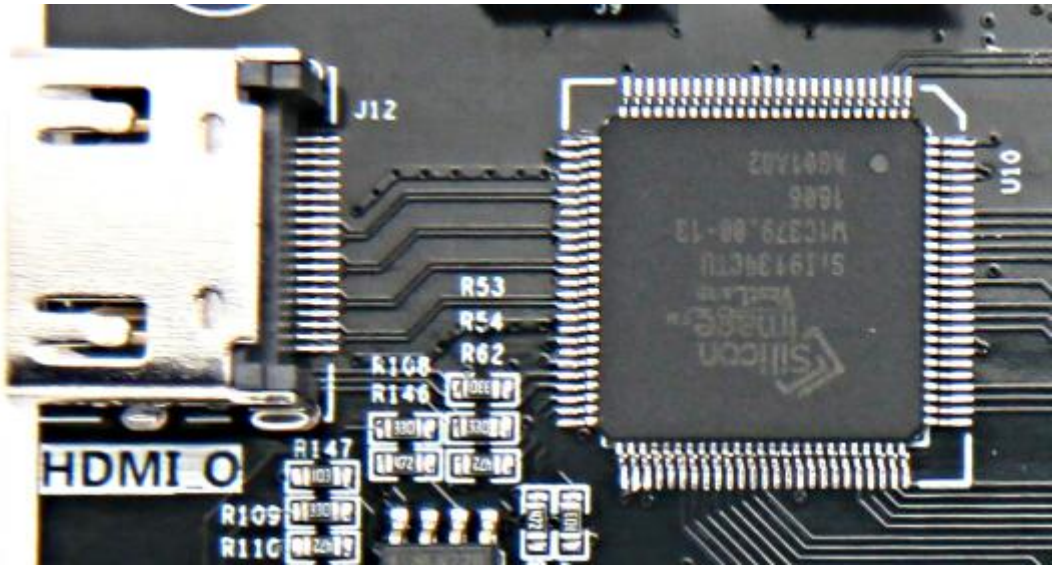


Figure 3-4-2 HDMI Output Connector on board

FPGA Pin Assignment：

Pins Name	FPGA Pins
9134_nRESET	J19
9134_CLK	M13
9134_HS	T15
9134_VS	T14
9134_DE	V13
9134_D[0]	V14
9134_D[1]	H14
9134_D[2]	J14
9134_D[3]	K13
9134_D[4]	K14
9134_D[5]	L13
9134_D[6]	L19
9134_D[7]	L20
9134_D[8]	K17
9134_D[9]	J17
9134_D[10]	L16
9134_D[11]	K16
9134_D[12]	L14
9134_D[13]	L15
9134_D[14]	M15
9134_D[15]	M16
9134_D[16]	L18
9134_D[17]	M18
9134_D[18]	N18
9134_D[19]	N19

9134_D[20]	M20
9134_D[21]	N20
9134_D[22]	L21
9134_D[23]	M21

5. HDMI Input Connector

The AX7103 used decoding chip SIL9013 HDMI of Silion Image company, supported input up to 1080P@60Hz, supported data output in various format. The IIC configure connector of SIL9013 connector to IOs of FPGA. To initialized and controlled the SIL9134 by FPGA program, HDMI Input connectors hardware designation as figure 3-5-1:

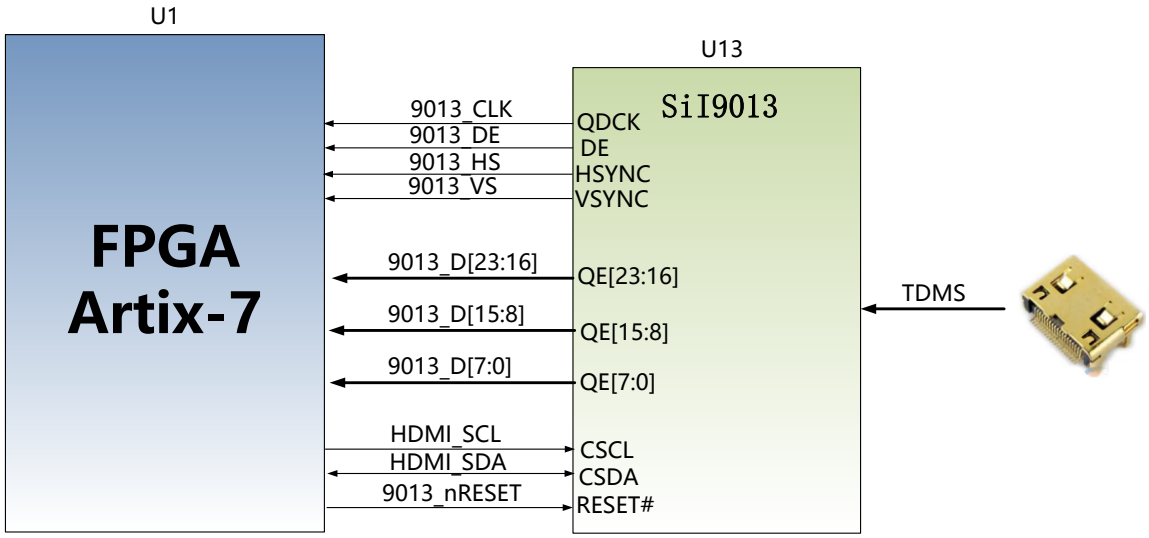


Figure 3-5-1 HDMI Input Schematic

HDMI Input connector on board, the picture as Figure 3-5-2:

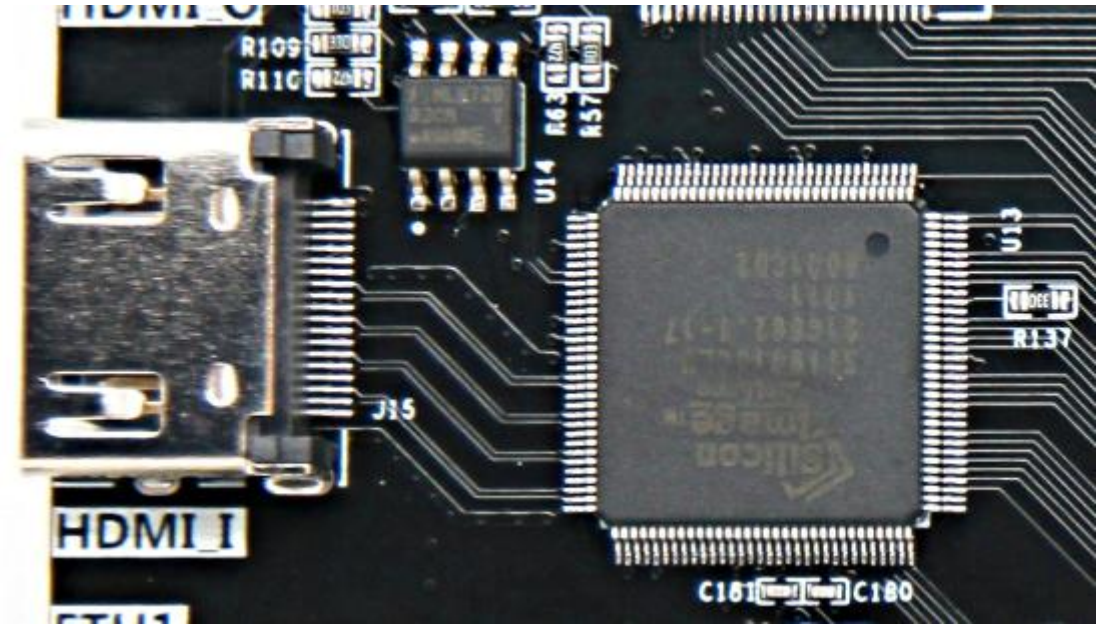


Figure 3-5-2 HDMI Input Connector on board

FPGA pins assignment：

Pin Name	FPGA Pins
9013_nRESET	H19
9013_CLK	K21
9013_HS	K19
9013_VS	K18
9013_DE	H17
9013_D[0]	H18
9013_D[1]	N22
9013_D[2]	M22
9013_D[3]	K22
9013_D[4]	J22
9013_D[5]	H22
9013_D[6]	H20
9013_D[7]	G20
9013_D[8]	G22
9013_D[9]	G21
9013_D[10]	D22
9013_D[11]	E22
9013_D[12]	D21
9013_D[13]	E21
9013_D[14]	B21
9013_D[15]	A21
9013_D[16]	F21
9013_D[17]	M17
9013_D[18]	J16
9013_D[19]	F15
9013_D[20]	G17
9013_D[21]	G18
9013_D[22]	G15
9013_D[23]	G16

6. SD socket

Many applications use a large external storage device, such as SD Card or CF card, for storing data. The AX7102 board provides the hardware needed for SD Card access. FPGA can access the SD Card in SPI mode and SD Card 4-bit or 1-bit mode. Figure 3-6-1 shows the related design of SD interface.

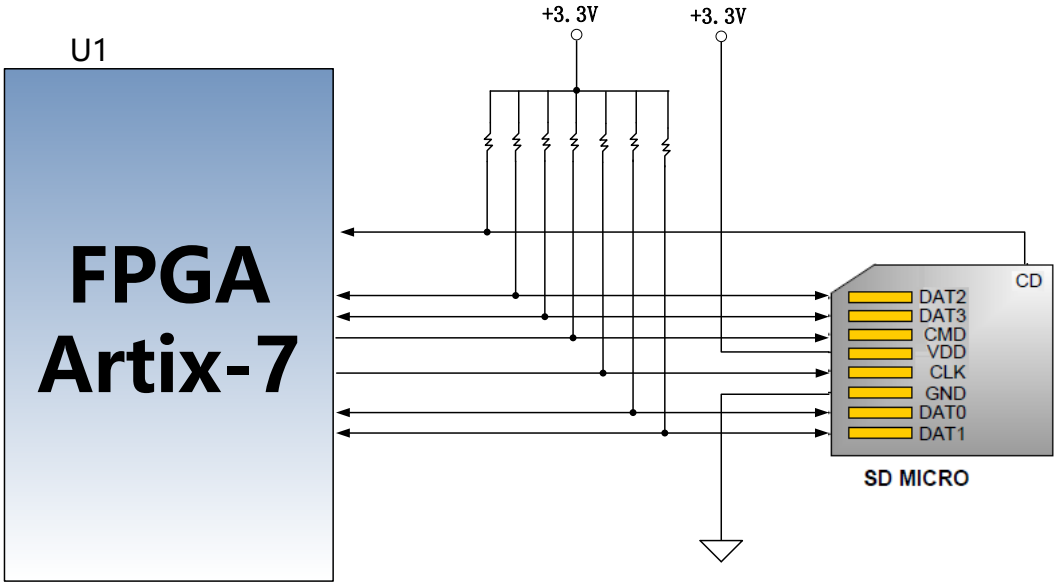


Figure 3-6-1 Design of SD Interface

Figure 3-6-2 shows the SD card socket on board.

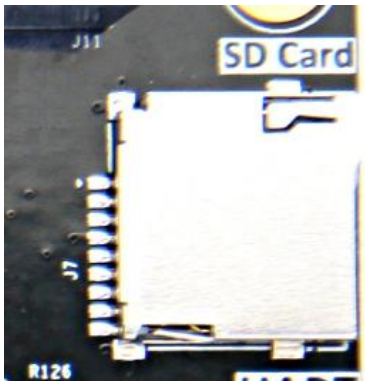


Figure 3-6-2 SD card socket on board

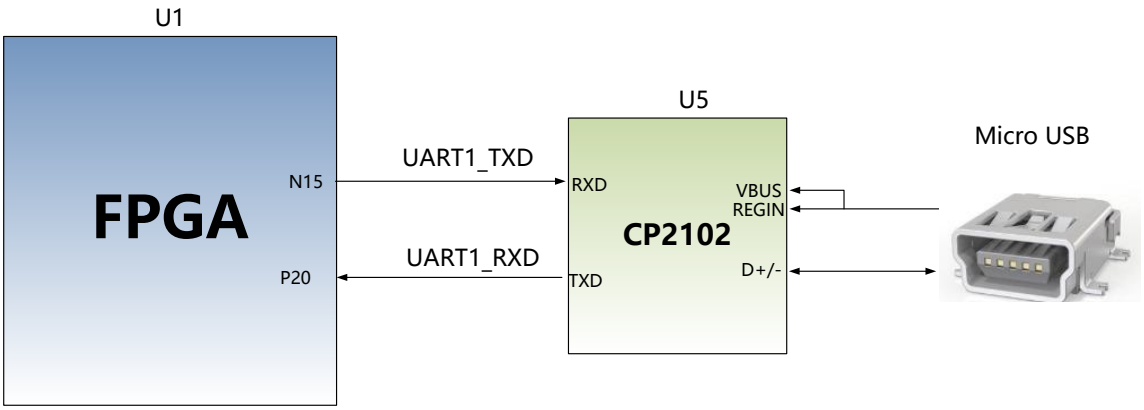
Pin Assignment of SD Socket

SD Mode	
Net Name	FPGA PIN
SD_CLK	AB12
SD_CMD	AB11
SD_CD_N	F14
SD_DAT0	AA13
SD_DAT1	AB13
SD_DAT2	Y13
SD_DAT3	AA14

7. USB Serial Port

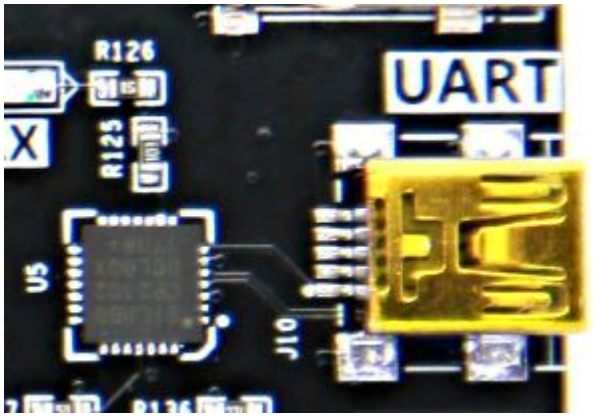
The board provides a MINI USB interface connector (J3) as a UART serial port to communicate with PC computer or other device. In AX7103 board, we use CP2102 chipset as an USB to UART bridge. When connecting an USB cable, FPGA

board can communicate with PC for UART communication. The hardware design of USB UART is showed as Figure 3-7-1.



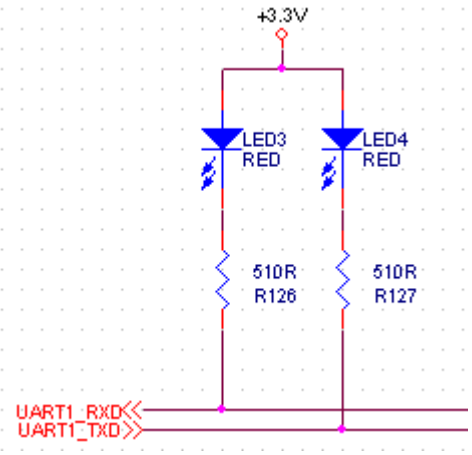
3-7-1 USB UART Interface

Figure 3-7-2 below shows the USB UART onboard.



3-7-2 USB UART onboard

There are two LEDs on board to indicate the UART operation status, the LED3 is used to indicate receiving status, and the LED4 is used to indicate sending status. The indication LEDs is design as Figure 3-7-3.



3-7-3 USB USB UART LED Indication

PIN Assignment of USB UART.：

Net Name	FPGA PIN
UART1_RXD	P20
UART1_TXD	N15

8. EEPROM 24LC04

The AX7103 used on chip of EEPROM, model 24LC04, Capacity of 4Kbit（2*256*8bit）comprise 2 blocks of 256byte, communication by IIC bus. EEPROM on board is to use to study IIC bus communication method. The I2C signal of EEPROM connected to BANK14 IO of FPGA. The figure 3-8-1 below showed the hardware designed schematic of EEPROM.

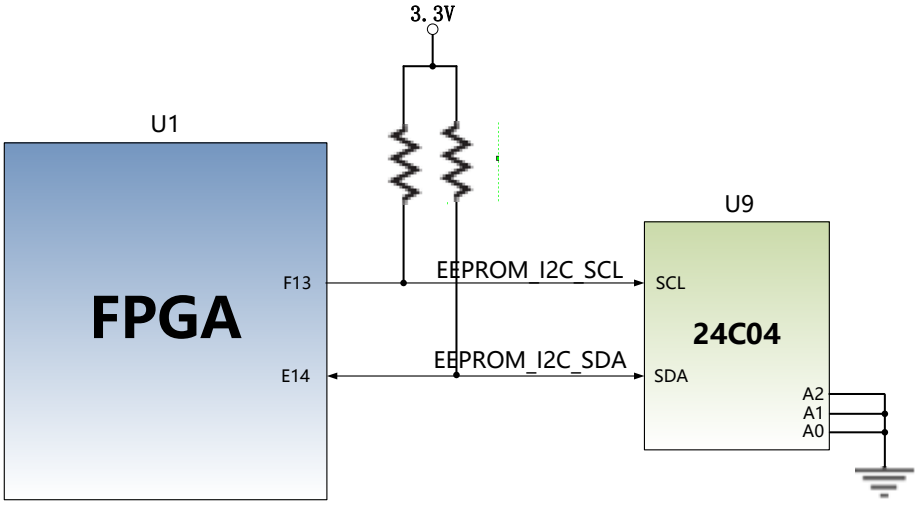


Figure 3-8-1 EEPROM hardware design schematic

Below figures shows the EEPROM on board.

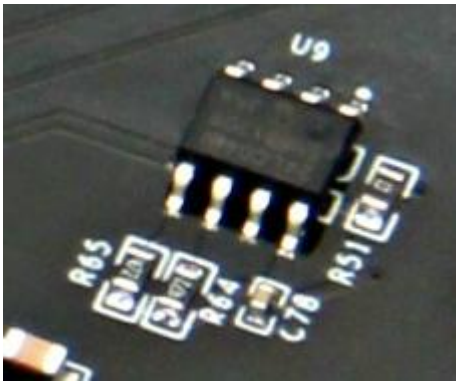


Figure 3-8-2 EEPROM on board

EEPROM pin Assignment：

Net Name	FPGA PIN
EEPROM_I2C_SCL	F13

EEPROM_I2C_SDA	E14

9. GPIO Expansion Headers

The expansion board reserved 2 pairs 2.54mm standard spacing 40-pin expansion header. They used to connect all kinds of AXSOC modules or outside circuit designed by users. There are 40pins for every expansion header, and one pin for 5V power supply, 2 pins for 3.3V power supply, 3 pins for ground, the other 34pins for IOs. Do not connected IOs to 5V circuit directly, avoid damage the FPGA, if to connect, that need through level convert chip.

33 ohms resistors in series between every IO pins of every expansion header and FPAG, to protect FPGA not damage by external over voltage or over current. Figure 3-9-1 below shows the circuit schematic of expansion header (J11).

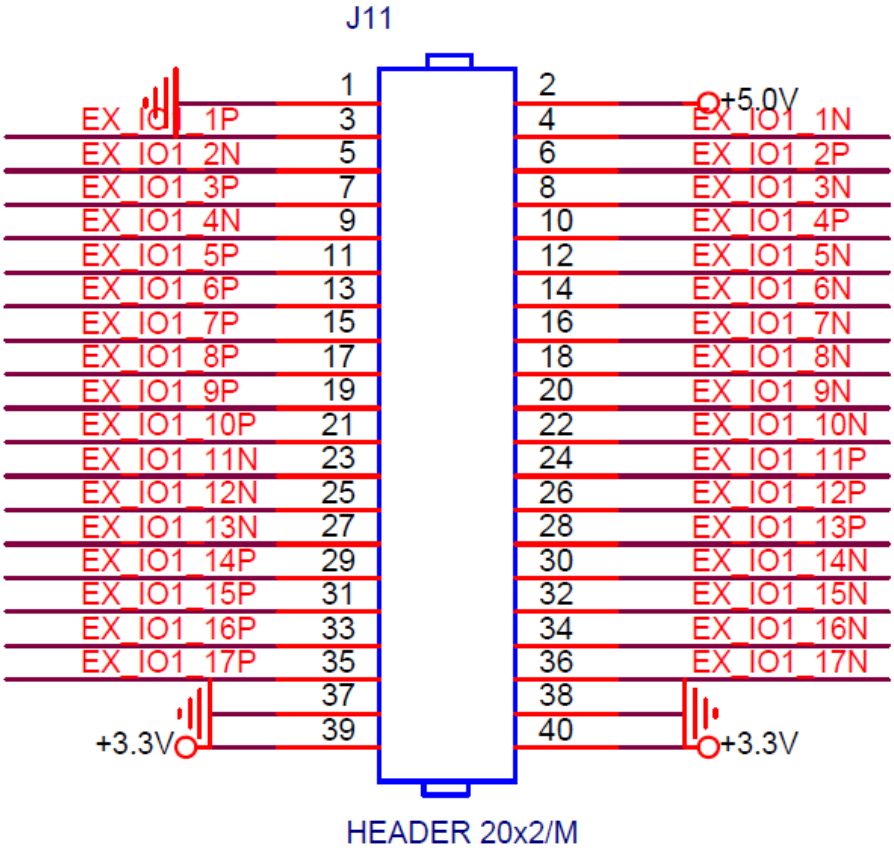


Figure 3-9-1 Schematic of Expansion header J11

Below picture is the J11 on board. Pin 1 and Pin2 marked on board.

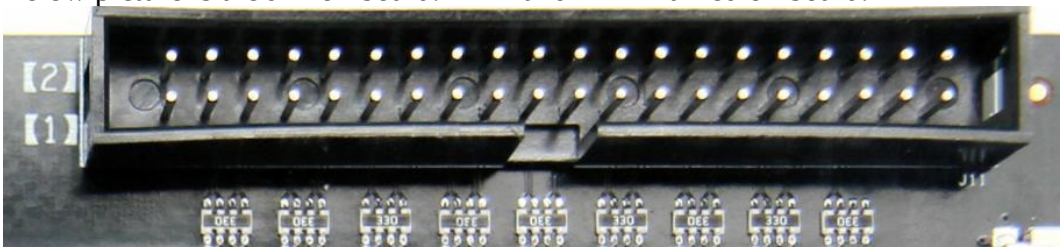


Figure 3-9-2 expansion header J11 on board

Pin Assignment of expansion header **J11**

J11 Pin	FPGA PIN	J11 Pin	FPGA PIN
1	GND	2	+5V
3	P16	4	R17
5	R16	6	P15
7	N17	8	P17
9	U16	10	T16
11	U17	12	U18
13	P19	14	R19
15	V18	16	V19
17	U20	18	V20
19	AA9	20	AB10
21	AA10	22	AA11
23	W10	24	V10
25	Y12	26	Y11
27	W12	28	W11
29	AA15	30	AB15
31	Y16	32	AA16
33	AB16	34	AB17
35	W14	36	Y14
37	GND	38	GND
39	+3.3V	40	+3.3V

Figure 3-9-3 below shows the circuit schematic of expansion header (J13).

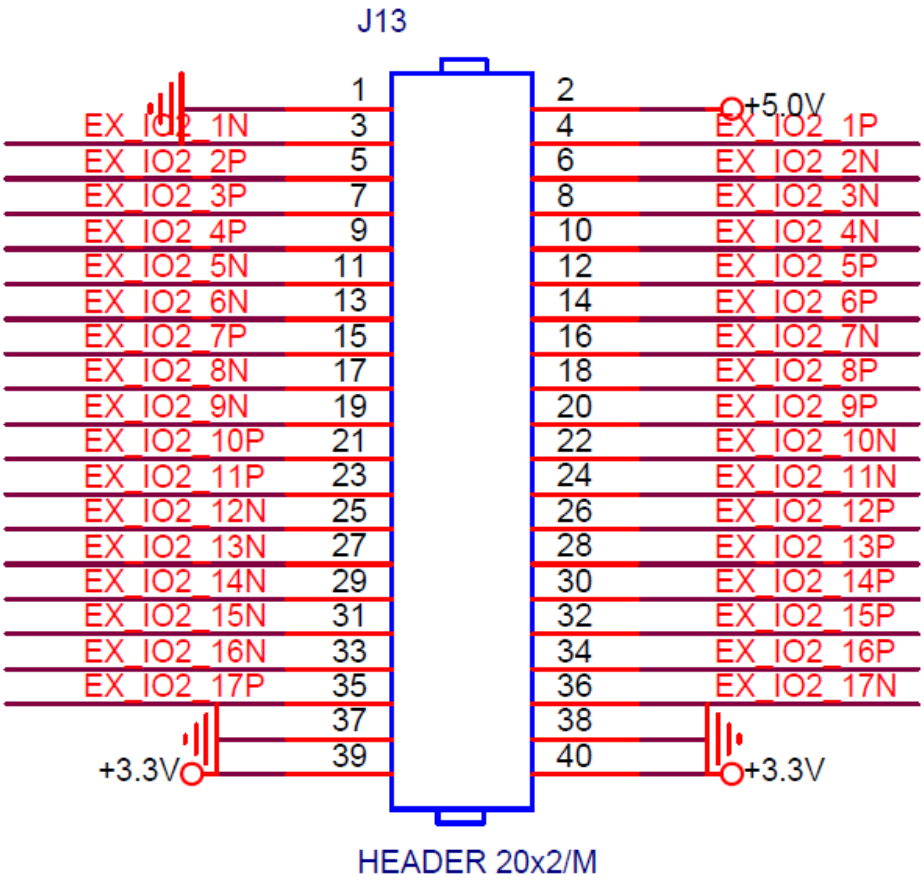


Figure 3-9-3 Expansion header J13 schematic

Below picture is the J13on board. Pin 1 and Pin2 marked on board.

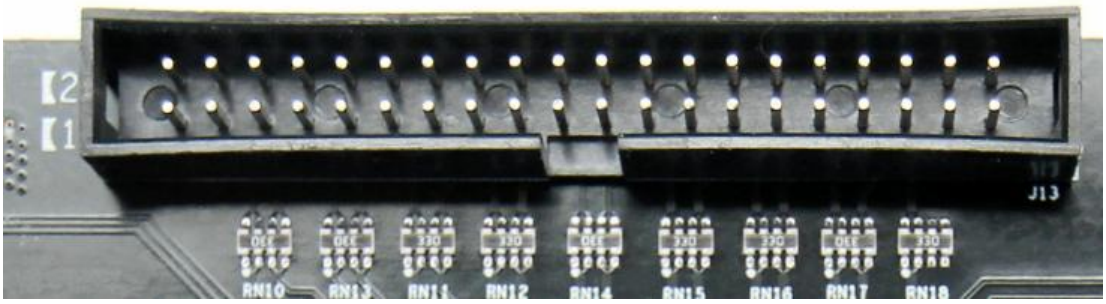


Figure 3-9-2 expansion header J13 on board

Pin Assignment of expansion header **J13**

J13 PIN	FPGA PIN	J13 PIN	FPGA PIN
1	GND	2	+5V
3	W16	4	W15
5	V17	6	W17
7	U15	8	V15
9	AB21	10	AB22
11	AA21	12	AA20
13	AB20	14	AA19

15	AA18	16	AB18
17	T20	18	Y17
19	W22	20	W21
21	T21	22	U21
23	Y21	24	Y22
25	W20	26	W19
27	Y19	28	Y18
29	V22	30	U22
31	T18	32	R18
33	R14	34	P14
35	N13	36	N14
37	GND	38	GND
39	+3.3V	40	+3.3V

10. JTAG Connector

The AX7103 Board reserves a 10Pin JTAG interface for downloading programs to FPGA QSPI FLASH. Each pin of JTAG interface on the expansion headers is connected to two diodes and a resistor that provides protection against high and low voltages. Figure 3-12-1 shows hardware design of JTAG interface.

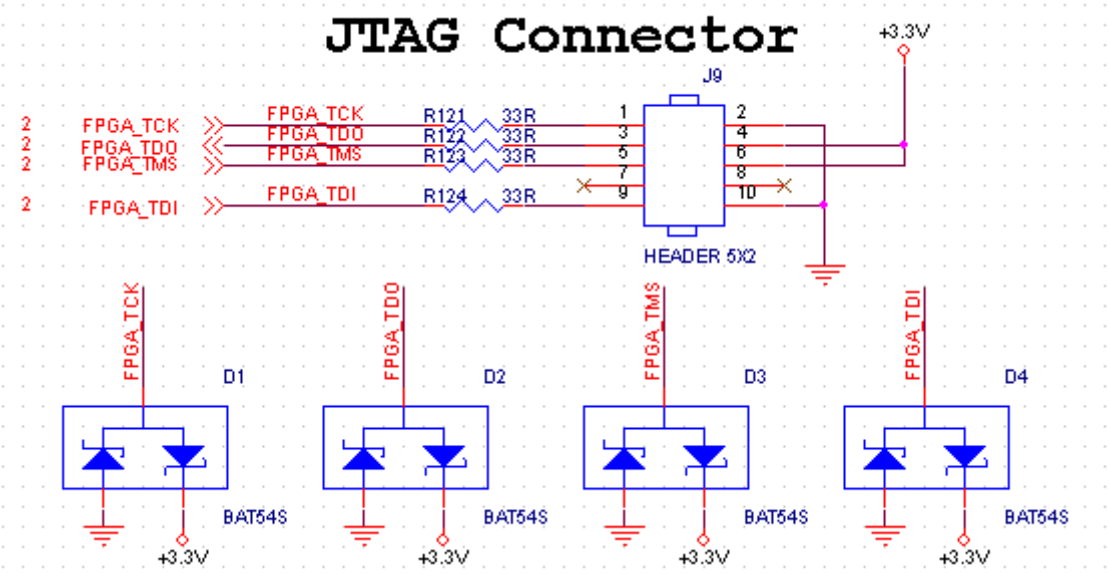


Figure 3-10-1 JTAG interface schematic

JTAG connector is standard 10pins connector, the pitch is 2.54mm. Figure 3-10-2 shows the onboard JTAG connectors. Do not hot swap

Figure 3-10-2 JTAG connector on board

11. XADC Connector（Not install by default）

AX7103 expansion board expanded XADC connector interface, the connectors used a 2x8 2.54mm pitch double-row pin. The XADC connectors expanded 3 pairs of ADC differential input connector, connected to 12-Bit 1Msps Analog to Digital Converter of FPGA. Included on pair of differential input connector, connected to dedicated differential analog input channel VP/VN of FPGA, The others twos connected to assisted analog input channel(analog channel 0 and 9) . Below figure 3-11-1 shows the Anti-aliasing filter circuit for 3 channels differential XADC input.

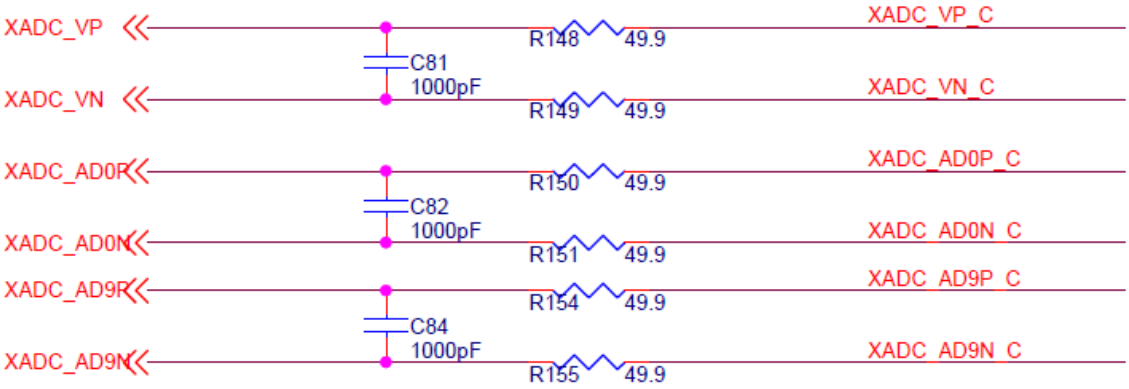


Figure 3-11-1 Anti-aliasing filter circuit

XADC connector circuit schematic as below figure 3-11-2:

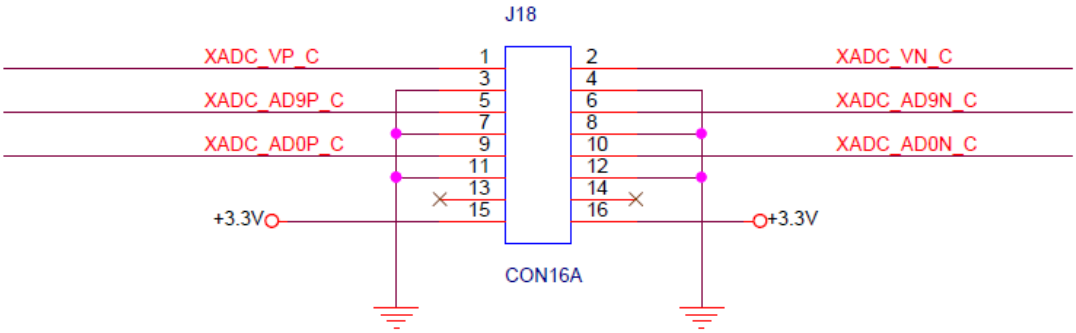


Figure 3-11-2 XADC Connector

Figure 3-11-3 is the picture of XADC on expansion board

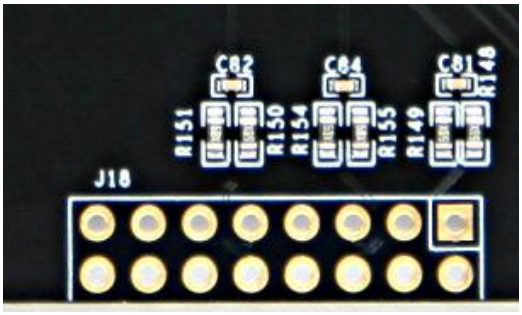


Figure 3-11-3 XADC on expansion board

Pin Assignment of XADC Connectors

XADC Connectors	FPGA PIN	Input magnitude	Description
1，2	VP_0 : L10 VN_0 : M9	Peak-to-Peak 1V	FPGA dedicated XADC input channel
5，6	AD9P : J15 AD9N : H15	Peak-to-Peak 1V	FPGA assisted XADC input channel 9（could use as normal IO）
9，10	AD0P : H13 AD0N : G13	Peak-to-Peak 1V	FPGA assisted XADC input channel 0（could use as normal IO）

12. Buttons

There are 2 user buttons KEY1~KEY2 on expansion boar, all connected to normal IOs of FPGA. When press down the buttons, will input low voltage to IOs of FPGA. When no press down the buttons, will input high voltage to IOs of FPGA. The buttons circuit schematic as below Figure3-12-1

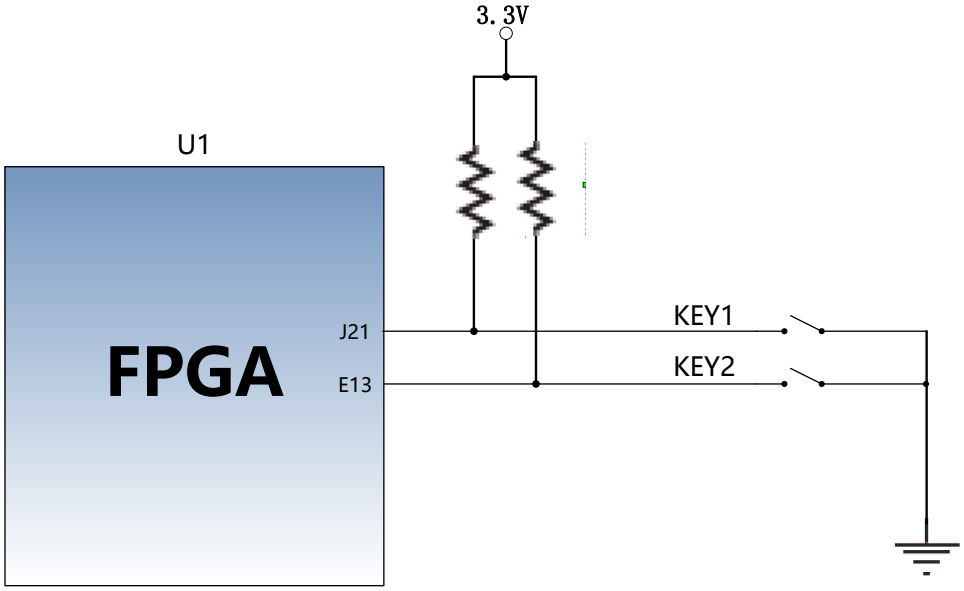


Figure 3-12-1 button hardware design schematic

Figure 3-12-2 are 2 user buttons on expansion board

Figure 3-12-2 2 user buttons on expansion board

Pin Assignment of Buttons.:

Net Name	FPGA PIN
KEY1	J21
KEY2	E13

13. LED

On expansion board ,there are 7 red led light, one for power indicator (PWR), two for USB Uart data receiver and transmission indicators, four for user LED light as normal IO（LED1~LED4）. The user LED will light on when low voltage output form FPGA IO, and the user LED will light off when high voltage output from FPGA IO, the power indicator will light on.

LED hardware design schematic as below figure 3-13-1

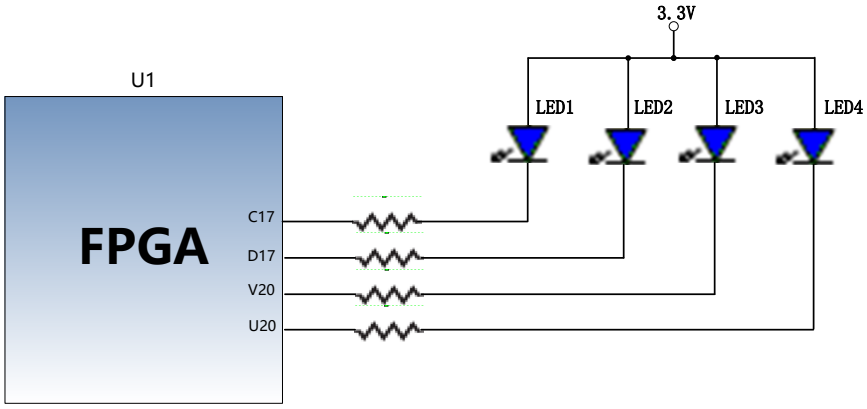


Figure 3-13-1 LED hardware design schematic

Figure 3-14-2 is the two user LEDs on expansion board

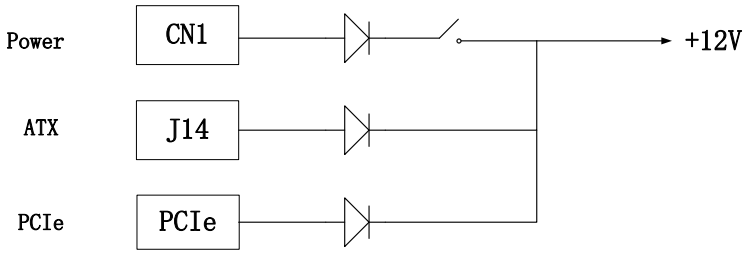
Figure 3-13-2 User LEDs on expansion board

Pin Assignment of User LEDs：

Net Name	FPGA PIN
LED1	B13
LED2	C13
LED3	D14
LED4	D15

14. Power Supply

The power supply of FPGA is DC12V， pls. use the certified adaptor. If the adaptor not certified that may damage the FPGA. The adaptor specification is DC12V. The FPGA also supported power from PCIe connector, and from chassis 12V supply directly.



On the expansion board, the power chip MP1482 could generate 4-channel supply, that are +5V, +3.3V,+1.8V and +1.2V. The +5V powered the Core board by board connectors. The power design schematics on expansion board, pls. refer to below figure 3-14-1

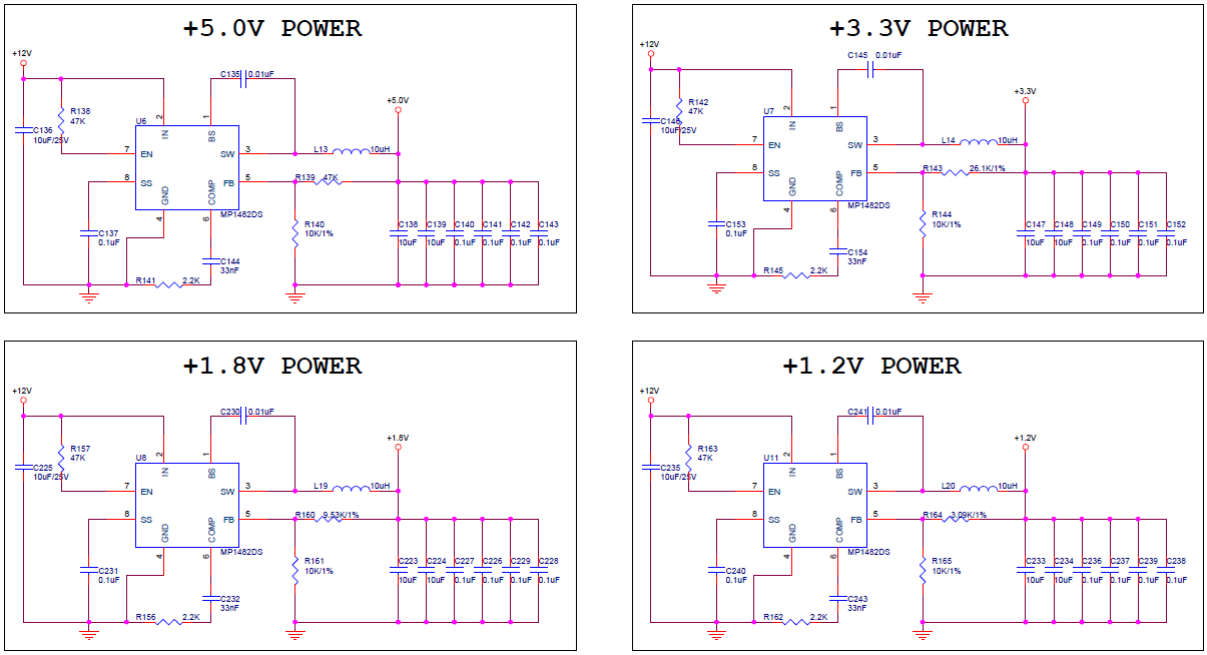


Figure 3-14-1 Power Schematic on expansion board

Figure 3-14-2 shows the DC/DC circuit on board

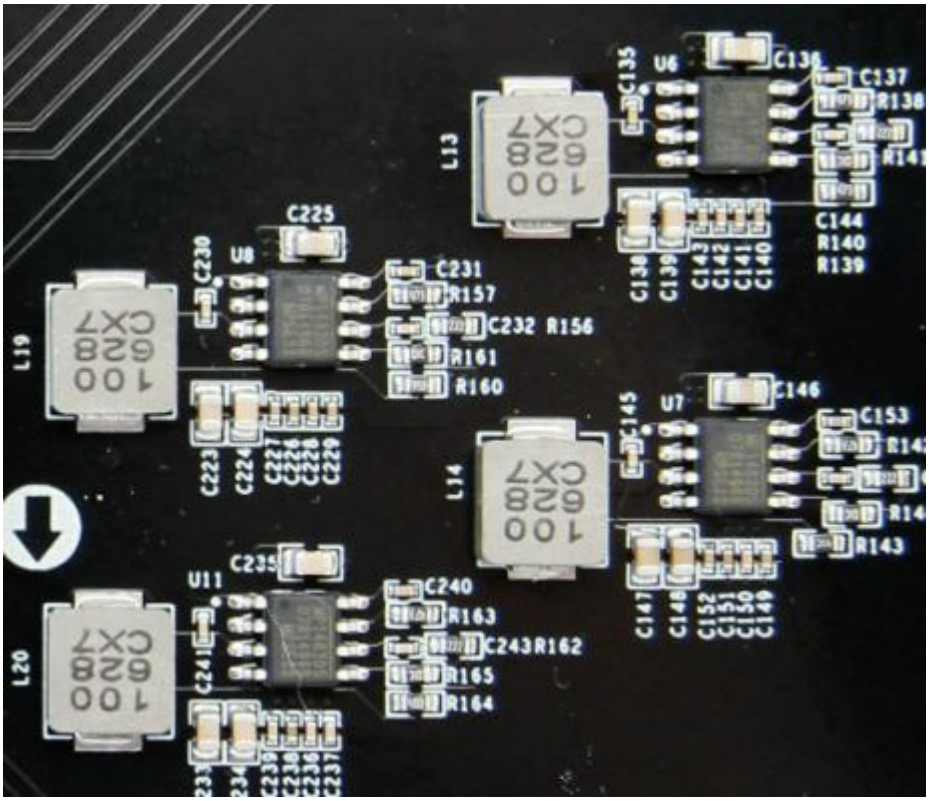


图3-14-2 DC/DC circuit on expansion board